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CONTROL DATA CORPORATION

CONTROL DATA®
DIGITAL OUTPUT UNIT
DA502-E,F,G,H,J,K

GENERAL DESCRIPTION
OPERATION AND PROGRAMMING
INSTALLATION AND CHECKOUT
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE
PARTS DATA

HARDWARE MAINTENANCE MANUAL

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MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

SHEET 1 OF 1

MANUAL REVISION	FCO OR ECO	EQUIPMENTS					
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A	DS13402	01	01	01	01	01	01
B	DS13223	—	—	—	—	—	—
	DS13544	—	—	—	—	—	—

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PREFACE

This manual describes the DA502-E through K Digital Output Unit (DOU) card, which plugs into the EL101-A Computer Interface Unit (CIU) or EL102-A Computer Interface Expander (CIE).

The following Control Data publications will be useful in installing and maintaining the DOU:

Description	Publication Number
1500 Product Family Index	88980000
EL101-A Computer Interface Unit/EL102-A Computer Interface Expander Manual	88980100
Key to Logic Symbols Manual	88981500
Input/Output Specification Manual	60165800
1700 Computer Reference Manual	60153100
SMM17 Version 3.0 Reference Manual, Test No. 90	60182000
Electromagnetic Compatibility Design Guide Handbook	CDC-STD-1-30.020

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Section One

GENERAL DESCRIPTION

1.1 GENERAL

This manual describes the Digital Output Unit (DOU) card which plugs into the Computer Interface Unit (CIU) or Computer Interface Expander (CIE). This manual is to be used in conjunction with the Computer Interface Unit/Computer Interface Expander Manual. The DOU may also be used with any other compatible real-time computer interface unit.

The DOU enables a control computer to activate external devices controlled through digital means in process control, manufacturing test, and medical computer applications. The unit provides 16 digital outputs held static until changed by the control computer. The outputs are logic level, 0 and +5 vdc as shown in Table 1.1. The outputs are limited to driving (sinking) 65 milliamperes when 0 vdc is the output.

The DOU has two modes of operation, asynchronous and synchronous, selectable by jumper on the card. Asynchronous mode allows the control computer to change the state of the outputs at any time. Synchronous mode enables the outputs to be synchronized with signals from an external device. This latter mode may be used to control data transfers from the DOU to an external device. The device may be one that requires data at specific intervals or one that contains data storage devices having a slow response time.

Table 1.1. DOU Assembly Configurations

EQUIP NO.	SIGNAL LEVELS (TYPICAL)	
	DATA OUTPUTS	SYNC INPUTS
DA502-E	True = 0v at 65 milliamperes False = +5v via 370 ohms	Logic level, 0v or +5v, true polarity selectable by jumper
DA502-F	True = +5v via 470 ohms False = 0v at 65 milliamperes	Logic level, 0v or +5v, true polarity selectable by jumper
DA502-G	True = 0v at 65 milliamperes False = +5v via 470 ohms	Form C contact closure
DA502-H	True = +5v via 470 ohms False = 0v at 65 milliampers	Form C contact closure
DA502-J	True = 0v at 200 milliamperes False = +28v external max.	Logic level 0v or +5v, true polarity selectable by jumper
DA502-K	True = +28v external max. False = 0v at 200 millamperes	Logic level 0v or +5v, true polarity selectable by jumper

1.2 PERFORMANCE/CHARACTERISTICS

1.2.1 PERFORMANCE

Requirements are:

- Number of outputs — 16 bits, one word
- Type — Logic levels, 0 vdc at 65 milliamperes or +5 vdc via 470 ohms. (Either polarity true within the set of 16 outputs.)
- Sync operation — Enables output word to be synchronized with signals from an external device.
- Interrupt flag — Occurs when using REQUEST sync input from an external device.
- Addressing capability — Unit may be connected into any station address location of the Computer Interface Unit (CIU) or Computer Interface Expander (CIE).

- Programming considerations — Data inputs, function outputs, or status inputs result in an internal reject. Sync mode will generate external reject when data output is attempted without request for data from an external device.
- Configuration — See Table 1.1 and Paragraph 1.3.

1.2.2 RELIABILITY

Requirements are:

- Mean time between failures (MTBF) - Estimated 75,000 hours
- Fail safe features - Inputs for synchronizing signals contain overload protection and will operate up to +70 vdc maximum. Damage may occur above +70 vdc.

1.2.3 MAINTAINABILITY

Maintainability provisions are:

- Mean time to repair (MTTR) - Estimated 0.5 hours
- Preventive maintenance - See Section Six
- Interchangeability - The DOU is a one-card device and may be interchanged with another identical version.
- Diagnostics available - SMM17 Diagnostic, Test 90 of the SMM17 Reference Manual may be used when the DOU is controlled by a CDC 1700/1770 computer. Section 9 of the test exercises reply, reject, and sync operation. Section 11 performs a closed-loop data test when a digital input unit (DIU) is connected to the DOU. Refer to the SMM17 Reference Manual.

- Special test equipment required - A digital input unit (Part No. 39842200) is required to perform closed-loop data testing with SMM17 Diagnostic, Test 90, Section 11. Refer to the SMM17 Reference Manual.

1.2.4 ELECTROMAGNETIC INTERFERENCE

The DOU is designed in accordance with the Electromagnetic Compatibility Design Guide Handbook.

1.3 EQUIPMENT CONFIGURATION

The DOU is a one-card device that can be inserted into any station address location in the CIU or the CIE. Table 1.1 illustrates the basic versions of the DOU. Paragraph 3.3 specifies the cabling required for connecting external devices to the DOU.

Section Two

OPERATION AND PROGRAMMING

2.1 CONTROLS AND OPERATING PROCEDURE

No controls provided.

2.2 JUMPERS AND OTHER EQUIPMENT CHANGES

2.2.1 MODE JUMPER

A jumper is provided to select asynchronous or synchronous mode operation. In the async mode, the control computer can change the state of the outputs at any time. In sync mode, the change of the output state is synchronized with signals from an external device, thus providing output changes at intervals specified by the external device.

2.2.2 NUT-AND-BOLT JUMPERS

Two jumpers are provided for selecting the input signal polarity on the request and reset sync signals from an external device. The H position represents a true input for signals going from 0 to +5 vdc. Position L represents a true input for signals going from +5 vdc to 0. See Figure 5.2 for configuration of Form C contact synchronizing signals.

One jumper is provided to select the output polarity of the ready signal to an external device. Position H provides a true output of +5 vdc. Position L provides a true output signal of 0 vdc (ground).

Two jumpers are provided to reset the output register by selecting either (or both) the master clear signal or the stall signal.

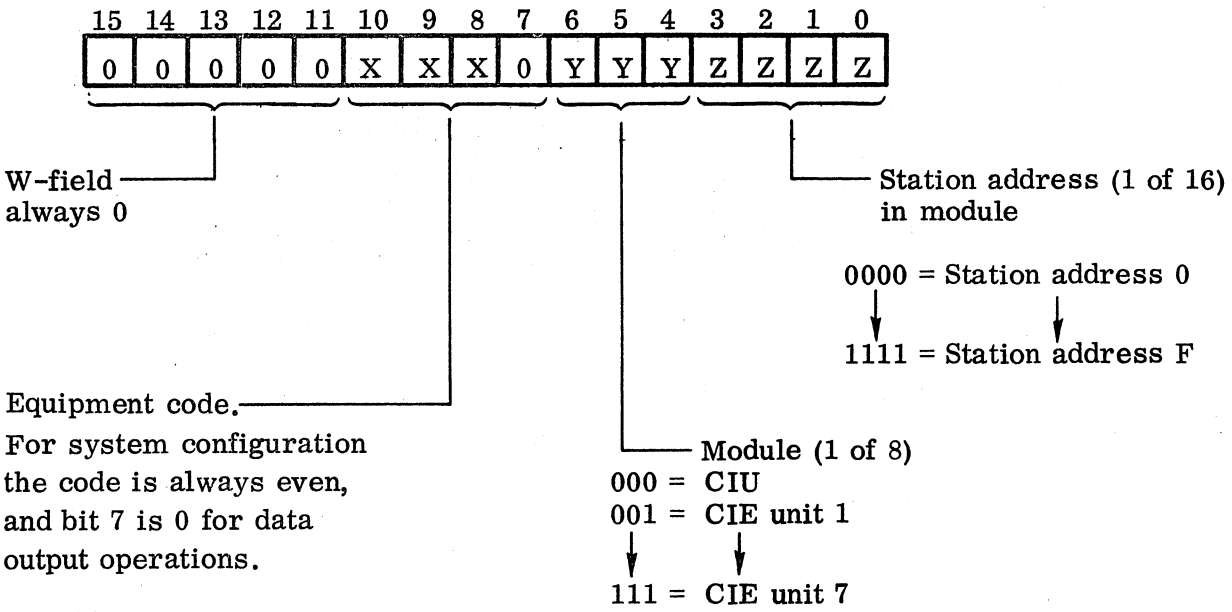
2.3 PROGRAMMING INFORMATION

2.3.1 DATA OUTPUT

The DOU responds to data output (computer write) operations only. The computer address must specify the station address location of the DOU in a CIU or a CIE.

The following CIU/CIE format is used:

Address



Example 1: A computer write to address $0607 will transfer data from the computer to a DOU located in station address 7 of a CIU on a system using equipment code C.

Example 2: A computer write to address $042B will transfer data from the computer to a DOU located in station address B of CIE module 2 on a system using equipment code 8.

Station addresses for the CIU and CIE may be found in Table 2.1 of the CIU/CIE Manual.

2.3.2 REJECTS

Internal rejects will occur is a data input, function output, or status input operation is attempted on the DOU.

An external reject will occur when the DOU is in sync mode and a data output is attempted before the unit is ready. This is because DOU has not received a sync request from an external device prior to the output operation.

2.3.3 INTERRUPT FLAG

The flag is generated upon receipt of the request sync signal from an external device. The interrupt flag remains active until a computer write operation loads the DOU with a new data word and resets the flag.

2.3.4 MASTER CLEAR

A computer console master clear will reset the DOU data register, set the interrupt flag signal and inhibit the ready signal to the external device.

2.3.5 STALL

A stall signal from the stall alarm unit will reset the DOU output data register, set the interrupt flag signal and inhibit the ready signal to the external device.

2.3.6 PROGRAMMING CONSIDERATIONS

The DOU does not respond to data input, function output, or status input operations.

Data output operations are always performed using the even equipment code number jumpered on the CIU control.

Section Three

INSTALLATION AND CHECKOUT

3.1 INSTALLATION REQUIREMENTS

The DOU is a one-card device 7-3/4 by 9 inches in size. It can be inserted into any station address location in the CIU, in a CIE, or any other compatible real-time computer interface unit. Signals are connected between the DOU and the external device by installing a cable on the rear of the CIU or CIE module in the respective station address location.

3.2 POWER REQUIREMENTS

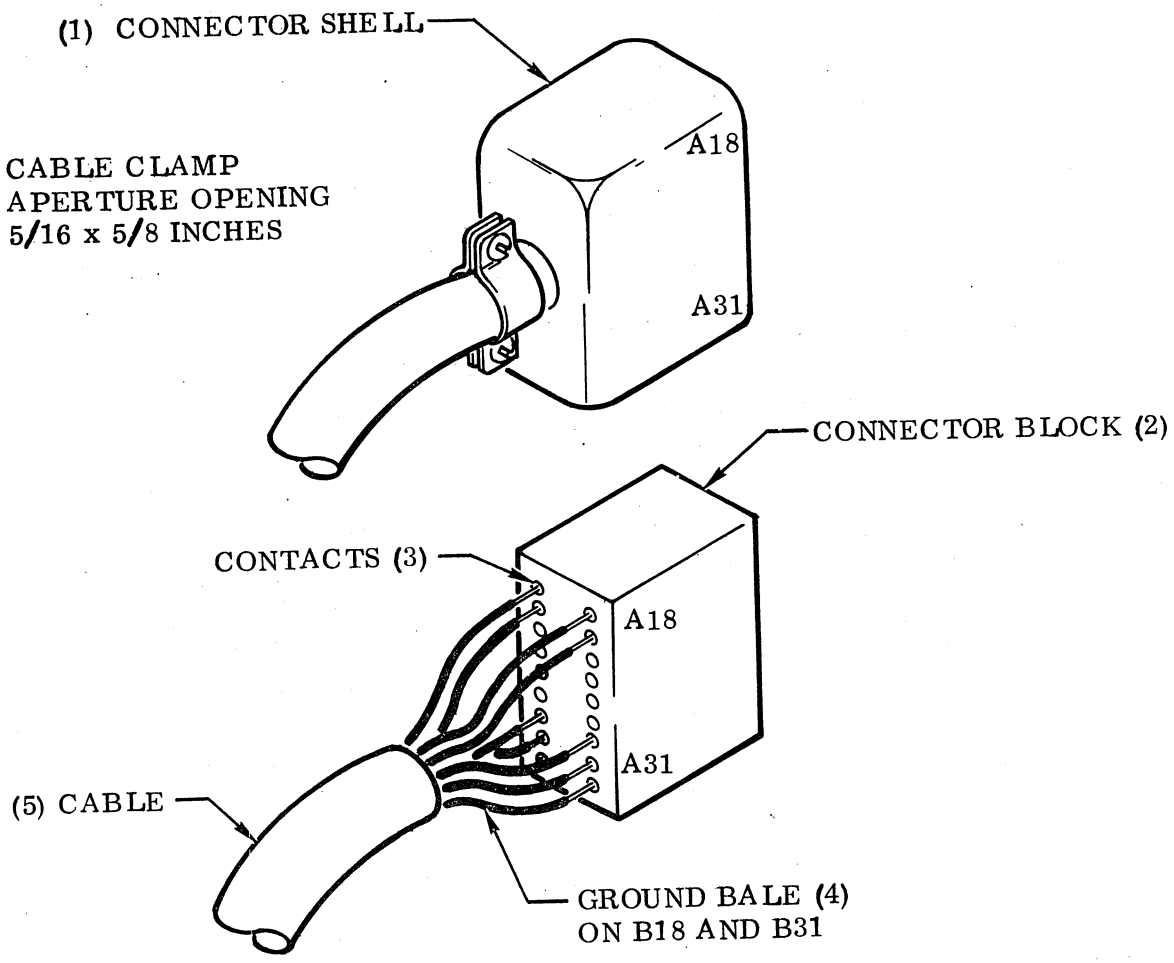
Logic power of +5 vdc is supplied by the CIU or CIE module. The current required by the DOU is 650 milliamperes. Input power for the CIU/CIE power supplies is 115 vac, 50/60 Hz. Power conversion transformer rack option 10299-22, is required in the system when input power is 220/240 vac, 50 Hz.

3.3 CABLING AND CONNECTORS

External signals are connected to the DOU by installing a customer-furnished cable assembly on the rear of the CIU or CIE module at the respective station address location. The connector shell, block, and contacts are supplied with each DOU. These are:

- Connector Shell - CDC Part No. 39498600
- Connector Block - CDC Part No. 94261810
- Contacts - CDC Part No. 94245600

A Berg Electronics, Inc., crimp tool No. HT-66 is required for connecting the contacts to the customer-furnished cable. Figure 3.1 illustrates a recommended assembly for the input cable.



ITEM	DESCRIPTION	CDC PART NO.	QUANTITY
1	Connector shell (28 pin)	39498600	1
2	Connector block	94261810	1
3	Contacts	94245600	21
4	Ground wire bale, solid 24AWG	(Furnished by customer)	As required
5	Cable, 19 twisted pair, 24AWG	(Furnished by customer)	As required

Figure 3.1. Input Cable Connector Assembly

3.4 INTERFACE CHARACTERISTICS

3.4.1 DATA/CONTROL BUS INTERFACE

The Data/Control Bus between the DOU and the CIU/CIE module is described in the Computer Interface Unit/Computer Interface Expander Manual.

3.4.2 EXTERNAL I/O INTERFACE

The signal and pin assignments for interfacing an external device are listed in Table 3.1.

3.4.2.1 Data Output Signal Levels

Requirements are:

- DA502-E and DA502-F (logic level)

  True = 0 to +0.5 vdc at 65 milliamperes

  False = +5 vdc via 470 ohms

- DA502-G and DA502-H (logic level)

  True = +5 vdc via 470 ohms

  False = 0 to +0.5 vdc at 65 milliamperes

- DA502-J (power driver)

  True = 0 to +0.5 vdc at 125 milliamperes

  False = Open collector to +28 vdc external load

- DA502-K (power driver)

  True = Open collector to +28 vdc external load

  False = 0 to +0.5 vdc at 125 milliamperes

Table 3.1. DOU External Interface

PIN NO.	SIGNAL	DESCRIPTION
A18	——	
B18	GND	Ground
A19	DB00	Output data bit 00
B19	DB01	01
A20	DB02	02
B20	DB03	03
A21	DB04	04
B21	DB05	05
A22	DB06	06
B22	DB07	07
A23	DB08	08
B23	DB09	09
A24	DB10	10
B24	DB11	11
A25	DB12	12
B25	DB13	13
A26	DB14	14
B26	DB15	Output data bit 15
A27	——	
B27	——	
A28	RESET	Sync reset to DOU
B28	READY	Ready from DOU
A29	REQST	Sync request to DOU
B29	——	
A30	——	
B30	——	
A31	——	
B31	GND	Ground

3.4.2.2 Request Input Signal

Characteristics are:

- DA502-E, DA502-F, DA502-J, and DA502-K (logic level)

  True = 0 to +0.4 vdc at 1.6 milliamperes

  False = +2.4 to 5.25 vdc

  Duration = 1 microsecond minimum

  Rise and fall times = Less than 100 nanoseconds for minimum duration signal.

- DA502-G and DA502-H (contacts) - The normally open terminal of isolated form C contacts. Reset generated by normally closed terminal (see Figure 5.2).

NOTE

A jumper is provided on the reset signal to select the opposite polarities for a true and false.

3.4.2.3 Reset Input Signal

Characteristics are:

- DA502-E, DA502-F, DA502-J, and DA502-K (logic level)

  True = 0 to +0.4 vdc at 1.6 milliamperes

  False = +2.4 to 5.25 vdc

  Duration = 1 microsecond minimum

  Rise and fall times = Less than 100 nanoseconds for minimum duration signal.

- DA502-G and DA502-H (contacts) - The normally closed terminal of isolated form C contacts. Request generated by normally open terminal (see Figure 5.2).

NOTE

A jumper is provided on the reset signal to select the opposite polarities for a true and false. The reset signal must be jumpered for a true when not used in sync mode.

3.4.2.4 Ready Output Signal

This signal is a logic level output as follows for all versions of the DOU:

True = 0 to +0.5 vdc at 65 milliamperes

False = +5, ±0.5 vdc via 470 ohms

Duration = 1 microsecond minimum; normally true until request is false and reset is true.

NOTE

A jumper is provided on the ready signal to select the opposite polarities for a true and false.

3.5 COOLING REQUIREMENTS

An air flow of 350 cfm is required across the DOU in system applications to assure adequate component life time. Standard air flow is provided when the DOU is inserted in a CIU/CIE system. Refer to the Computer Interface Unit/ Computer Interface Expander Manual.

3.6 ENVIRONMENTAL LIMITATIONS

Refer to Paragraph 3.6 of the Computer Interface Unit/Computer Interface Expander Manual.

3.7 PREPARATION FOR USE

Verify mode jumper is proper position.

Verify request, reset and ready signal jumpers select proper polarity for system operation in sync mode.

Verify reset signal jumpered for true (position H) if not used in system application.

Verify proper position of master clear and stall jumpers.

Section Four

THEORY OF OPERATION

4.1 GENERAL

The DOU, connected in a CIU or CIE , enables a control computer to generate digital output signals for external equipment. The DOU provides logic level signal conditioning for the output signals. It provides the logic level or contact closure signal conditioning for the external synchronizing signals. The DOU also provides control logic for communicating with the CIU/CIE. The DOU is a data output device only and provides no status or function capability.

Figure 5.1 is a simplified block diagram and Table 4.1 defines the signal mnemonics and terms. Figure 5.6 is the logic package for the DOU.

4.2 PRINCIPLE OF OPERATION

Operation of the DOU can be either asynchronous mode or synchronous mode. In the asynchronous mode, the control computer can change the state of the outputs at any time. In the synchronous mode, the change of the output state is controlled by synchronizing signals from the external device. When data is loaded into the DOU, the state of all 16 outputs (bits) are changed according to the computer data word.

In the following descriptions, a logical 1 is +2.4 to 5.25 vdc, a logical 0 is 0.4 vdc or less, and the timing tolerances are ±25%.

4.2.1 SIGNAL CONDITIONING

4.2.1.1 Data Output Signals

The DOU provides signal conditioning circuits for logic level outputs to the external device. Each circuit provides +5 vdc via 470 ohms when a logical 1 is

required for a true output. The circuits provide 0v at 65 milliamperes when a logical 0 is required for a true output. See Table 1.1 for the signal input/output assemblies.

4.2.1.2 External Sync Signals

Jumpers are provided for selecting the proper input/output polarities for external synchronizing signals.

- Request - A signal from the external device to the DOU requesting a data output. The circuit responds to a logical 1 as a true input when the jumper is in position H. A logical 0 is a true input when the jumper is in position L.
- Ready - A signal from the DOU to the external device indicating that a data value is ready in the data register. The jumper in position H provides a logical 1 for a true output. Position L provides a logical 0 as a true output.
- Reset - A signal from the external device to the DOU resetting the sync logic. (This signal is not always used.) The jumper in position H responds to a logical 1 as a true input. Position L responds to a logical 0 as a true input.

NOTE

When no reset input signal is connected to the DOU, the reset jumper must be placed in position H for proper sync operation.

4.2.2 ASYNCHRONOUS MODE OPERATION

Data is loaded in the DOU when a write operation is performed by the computer to the DOU station address. The data transfer sequence is illustrated in Figure 5.3 and occurs as follows:

- The REPLY/REJECT FF is placed in the REPLY state when the DOU is not active.
- The DOU connects to an output operation when the station select signal (TP20) becomes a logical 1 and signal FUSTF remains a logical 1 on the bus.
- Upon receipt of a write signal (TP29 becomes a logical 1), the DOU loads the data register with the information from the computer data lines. The data is presented to the external device and a reply is sent to the computer.
- The output operation is terminated when the write (TP29) and station select (TP20) return to a logical 0. The REPLY/REJECT FF remains in the REPLY state since an external reject is never generated in asynchronous mode.

The request and reset inputs are not used in asynchronous mode. A one microsecond ready signal, denoting output data is available, is sent to the external device when the jumper on the reset signal is in the H position.

4.2.3 SYNCHRONOUS MODE OPERATION

4.2.3.1 Sync Reply Sequence

Data transfers in synchronous mode are controlled by the external device. The data transfer reply sequence, using logic level synchronizing signals, is illustrated in Figure 5.4 and occurs as follows:

- The external device sends a request (TP31 becomes logical 1) to the DOU when data is required. The reset signal (TP24) drops to logical 0 when used.

- The request input sets the INT/SYNC FF (TP18 becomes logical 1). The DOU flag (FLXXF) is sent to the CIU/CIE control, which in turn generates an interrupt to the computer. A write cycle is then initiated upon receipt of the interrupt.

- The computer sends a data word to the DOU, which responds to the write command when station select (TP20) becomes a logical 1. Signal FUSTF remains a logical 1.

- The write signal (TP29 logical 1) triggers the LOAD DATA one-shot (TP27). The computer data is loaded into the DOU data register and a reply is sent to the computer. The write operation is terminated when station select (TP20) and write (TP29 return to a logical 0. The REPLY/REJECT FF remains in the REPLY state.

- After the DOU data register is loaded, ready signal (TP17 logical 1) is sent to the external device, signifying data is now available.

- The external device examines the data and makes request false (TP31 logical 0) if it is not already false. Also, reset becomes true (TP24 logical 1) if it is being used.

- The ready signal remains true until the request signal from the external device is false and the reset signal is true (if used).

The reset signal permits the external device to control the reset of the synchronizing logic after an input operation. It is used when synchronizing from relay contacts or logic level signals that do not settle in one microsecond. On contact synchronization, the request and reset signals are generated by opposite sides of the form C contacts. See Figure 5.2.

When the reset signal is not connected to the DOU, the jumper for reset control is placed in the H position. The ready signal to the external device is then present for either:

- Approximately one microsecond when the request signal input is a pulse of one-microsecond duration; or
- Remains true until request drops (where the ready signal is used to drop request).

4.2.3.2 Sync Reject Sequence

The DOU is normally not ready for data transfers in sync mode. If the computer initiates a data transfer prior to the DOU receiving a request from the external device, the DOU sends a reject to the computer. The reject sequence is illustrated in Figure 5.5 and occurs as follows:

- No request is received from the external device; therefore, the INT/SYNC FF is not set (TP18 logical 0).
- The station select signal (TP20 logical 1) enables REJECT ENABLE one-shot that sets the REPLY/REJECT FF to the REJECT state.
- When the write signal (TP29 logical 1) is received, a reject is sent to the computer. The REJECT state also inhibits sending a ready signal to the external device.
- The reject sequence terminates when write (TP29) and station select (TP20) return to a logical 0. The REPLY/REJECT FF is set to the REPLY state, ready for the next transfer operation.

4.2.4 ASYNCHRONOUS MODE WITH INTERRUPT

When the DOU is operated in async mode, the request input signal can be used to generate a flag (interrupt) to the computer. The sequence is identical to

the sync mode reply sequence, but the computer can initiate and complete a data transfer with or without a request being present. The REJECT ENABLE one-shot that places the REPLY/REJECT FF in the REJECT state is never enabled. The DOU, therefore, always sends a reply to the computer.

4.2.5 MASTER CLEAR OR STALL

The DOU does not contain a programmable master clear. A computer console master clear or stall will set the INT/SYNC FF and the output data register. The master clear will reset the READY FF and inhibit sending a ready to the external device.

Table 4.1. Glossary of Terms

TERM	DEFINITION
DB00F - DB15F	Data bits 00 - 15 false (from CIU/CIE common bus)
DB00 - DB15	Output data bits 00 - 15 (to external device)
MCLRF	Master clear false (from bus)
READF	Read false (from bus)
FUSTF	Function/status false (from bus)
SSXXF	Station select false (from bus)
FLXXF	Flag line false (to bus)
RPLYF	Reply false (to bus)
RJCTF	Reject false (to bus)
REQST	Request sync (from external device)
READY	Ready (to external device)
RESET	Reset sync (from external device)
STALF	Stall signal (from stall alarm unit)

Section Five

DIAGRAMS

5.1 GENERAL

This section contains the following diagrams:

Figure No.	Title
5.1	Digital Output Unit Block Diagram
5.2	Form C Contract Closure Synchronizing Signals
5.3	Asynchronous Mode Reply Sequence
5.4	Synchronous Mode Reply Sequence
5.5	Synchronous Mode Reject Sequence
5.6	Digital Output Unit Logic Package

5.2 DIAGRAMS

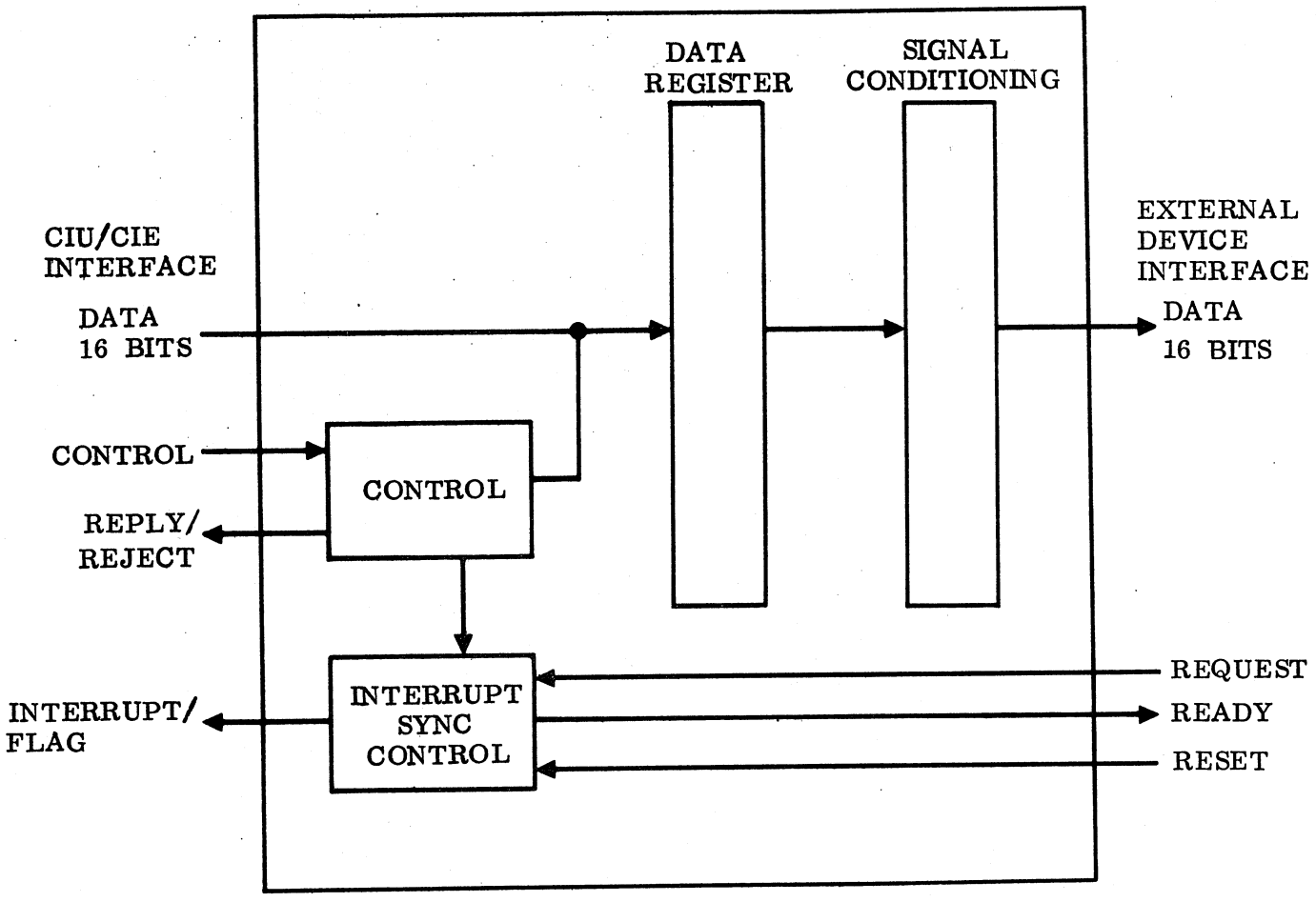


Figure 5.1. Digital Output Unit Block Diagram

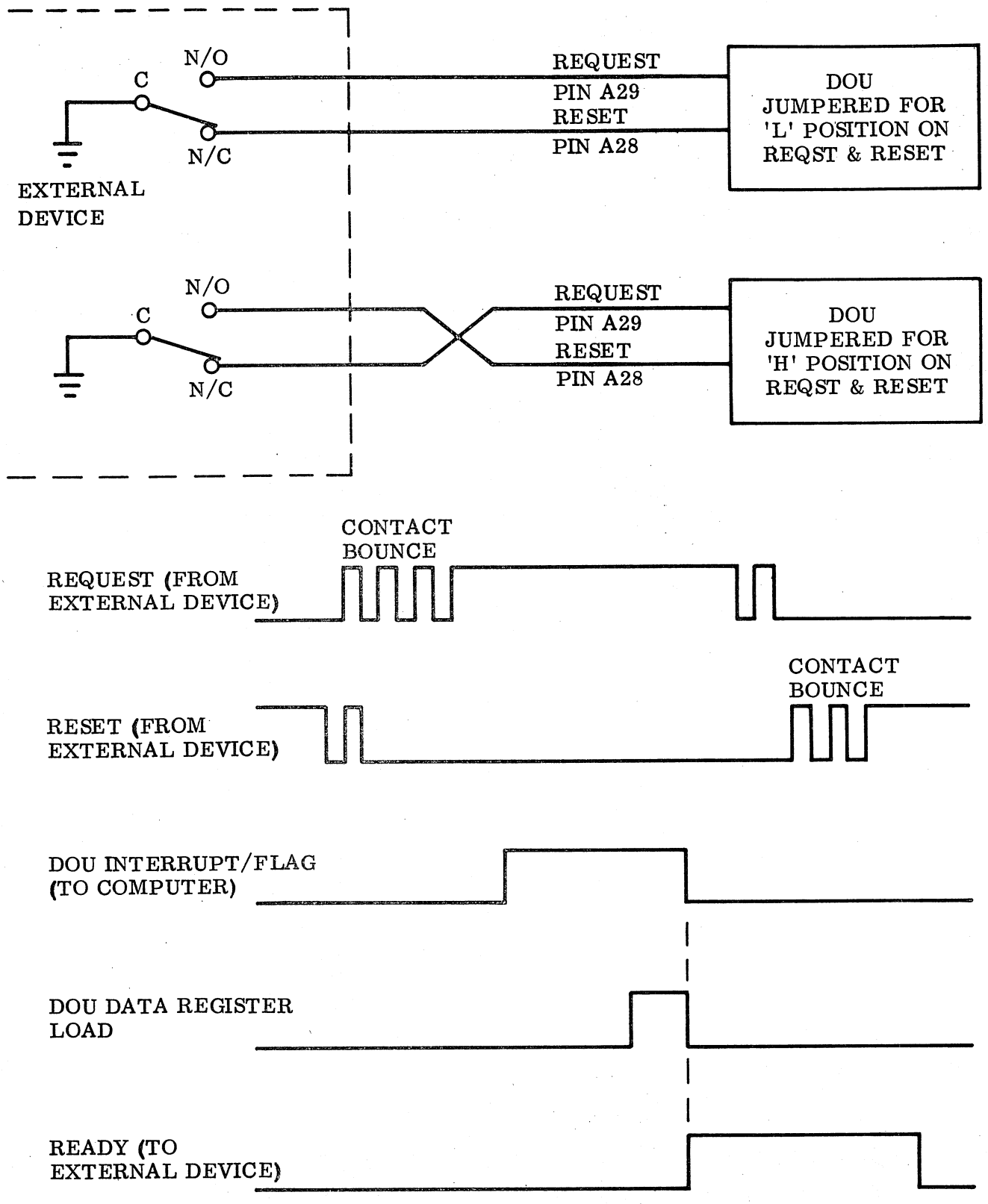


Figure 5.2. Form C Contact Closure Synchronizing Signals

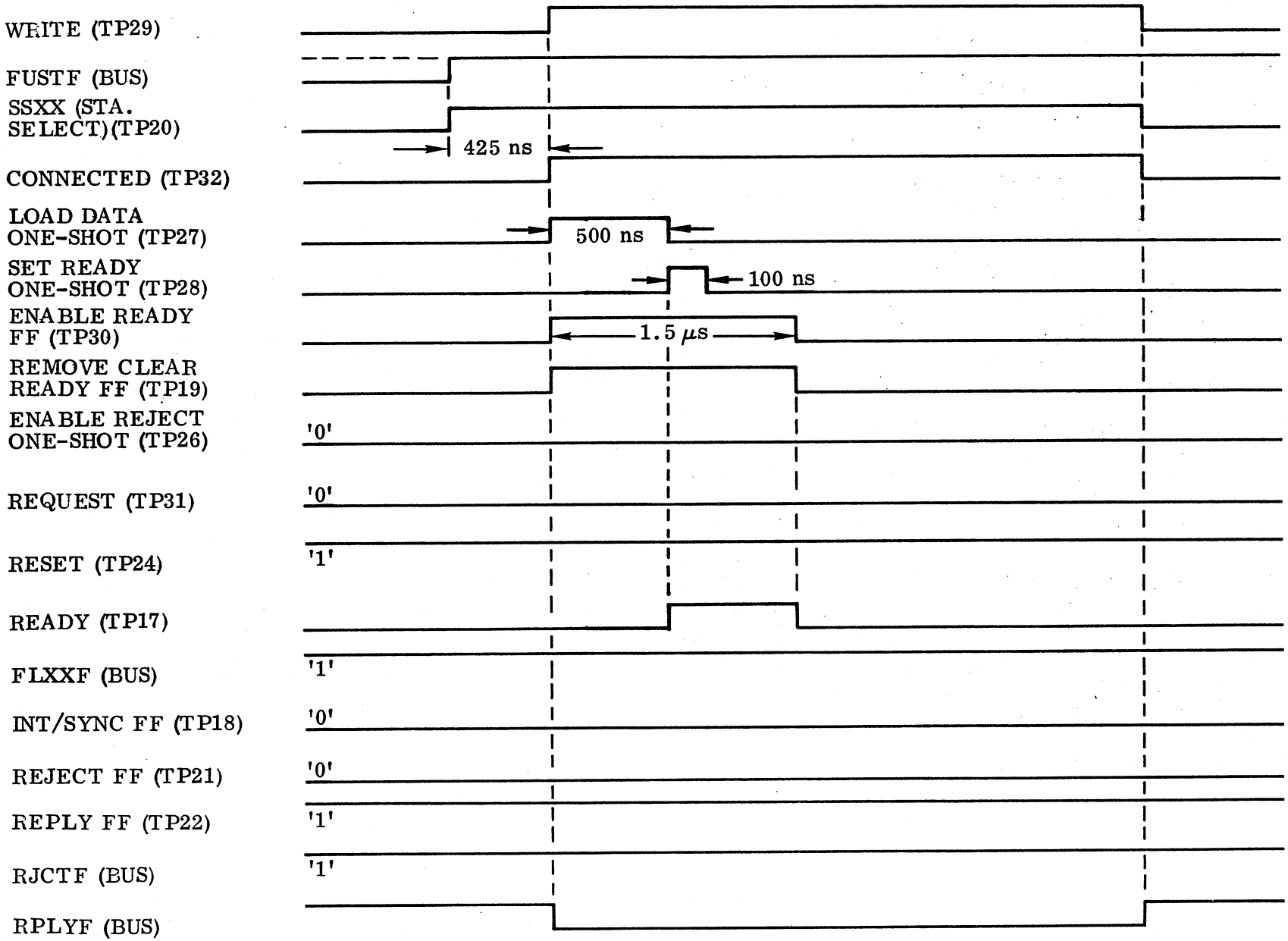


Figure 5.3. DOU Asynchronous Mode Reply Sequence

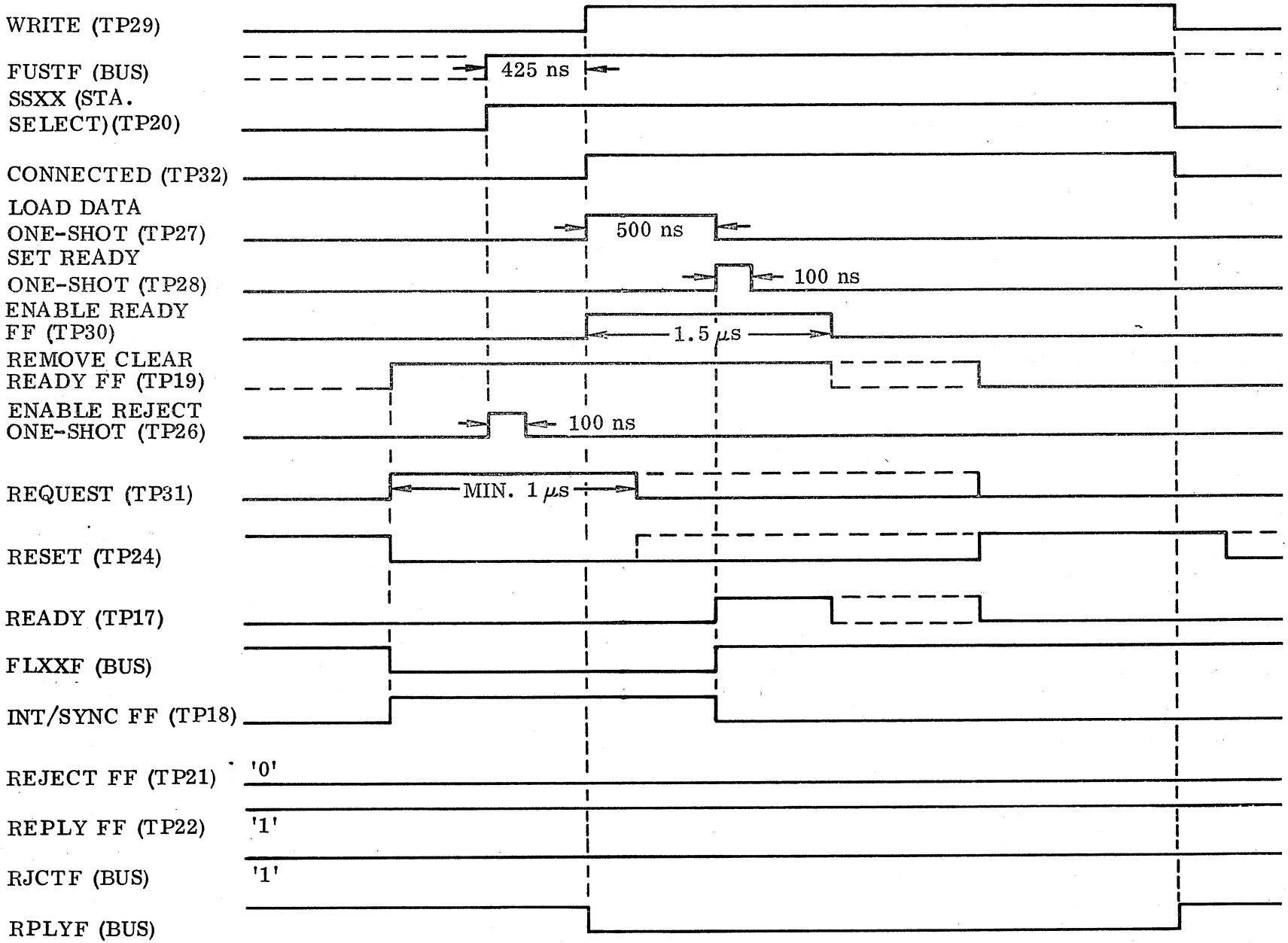


Figure 5.4. DOU Synchronous Mode Reply Sequence

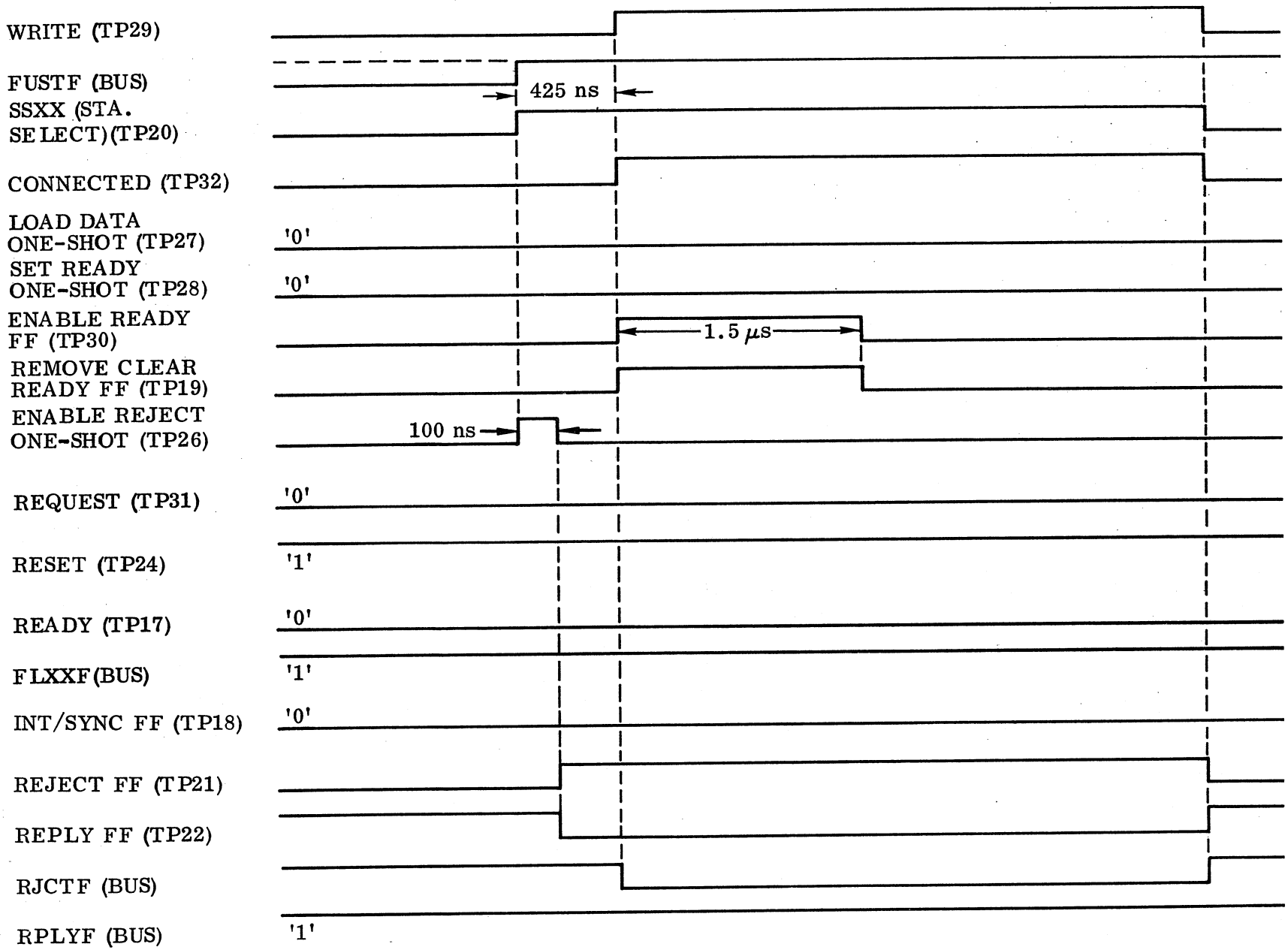
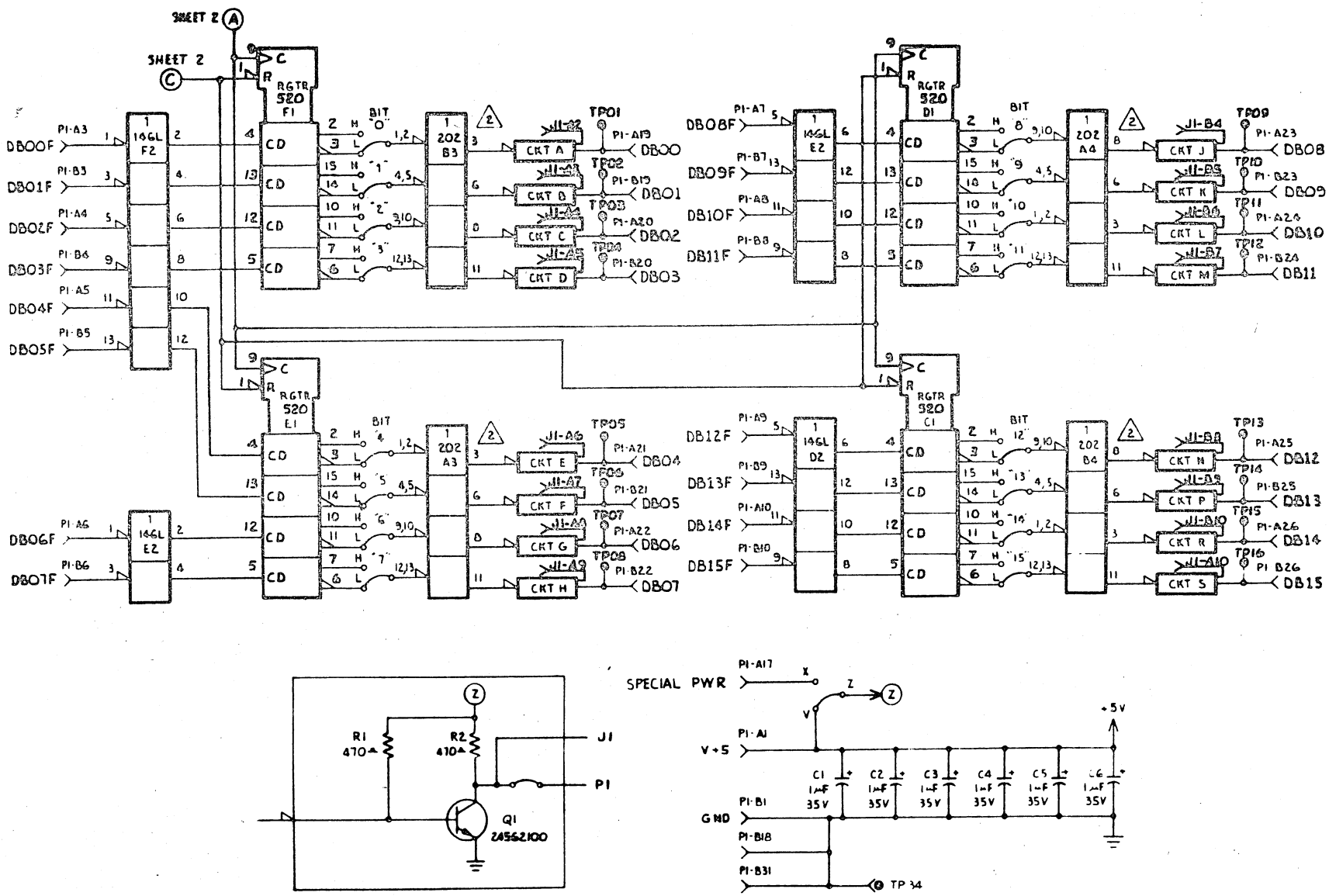


Figure 5.5. DOU Synchronous Mode Reject Sequence

Figure 5.6. Digital Output Unit Logic Package



DISCRETE CKT (TYP A THRU T)

4. P.W. BOARD HAS CAPABILITY TO ADD (2) CAPACITORS.
3. FOR KEY TO SYMBOLS SEE DWG 88921500.
2. ALL ELEMENT IDENTIFIER 202 & 203 ARE OPEN COLLECTOR.
1. ALL RESISTORS ARE 1/4 W.

NOTES UNLESS OTHERWISE SPECIFIED

DR 88800200 DETACHED LIST

	A	B	C	D	E	F
1			74175	74175	74175	74175
2				74L04	74L04	74L04
3	7403	7403				
4	7403	7403				
5						
6		7400	7474	7474	7409	74L06
7	840	840	7413	7413	7003	7405

LOGIC TITLE: DIGITAL OUTPUT UNIT — TRUE = 0V @ 65 MA, LL SYNC

LOGIC DWG NO: 88800200 SH 1 THRU 2 REV C

PCB NO: 88800100 PCB NO: 88800000

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif 92037

FIRST USED ON	DAS02	
DR	T. Lyman	6-13-73
CHK		7-25-73
ENGR		7-26-73
MGR		
APPD		9/7/73

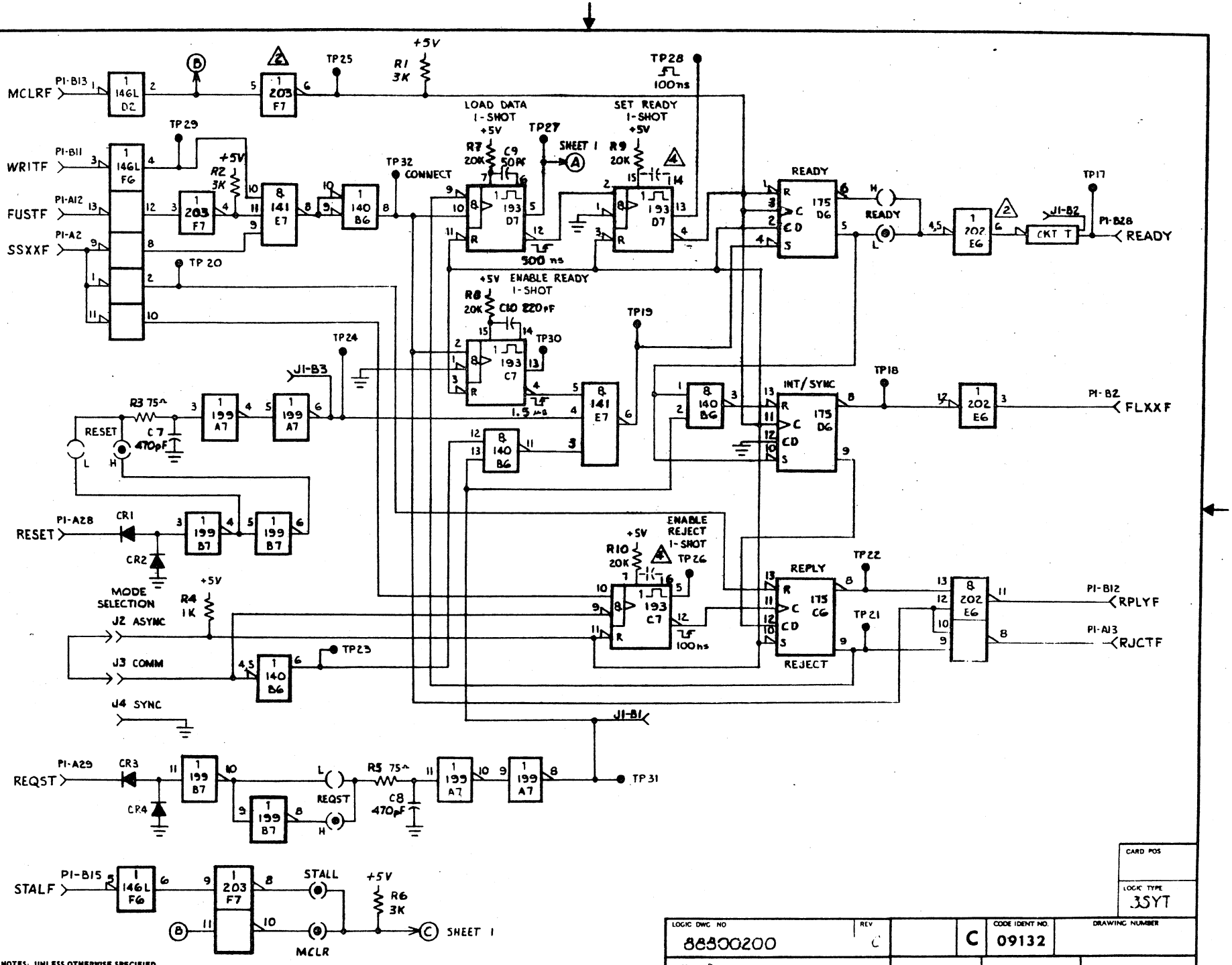
TITLE

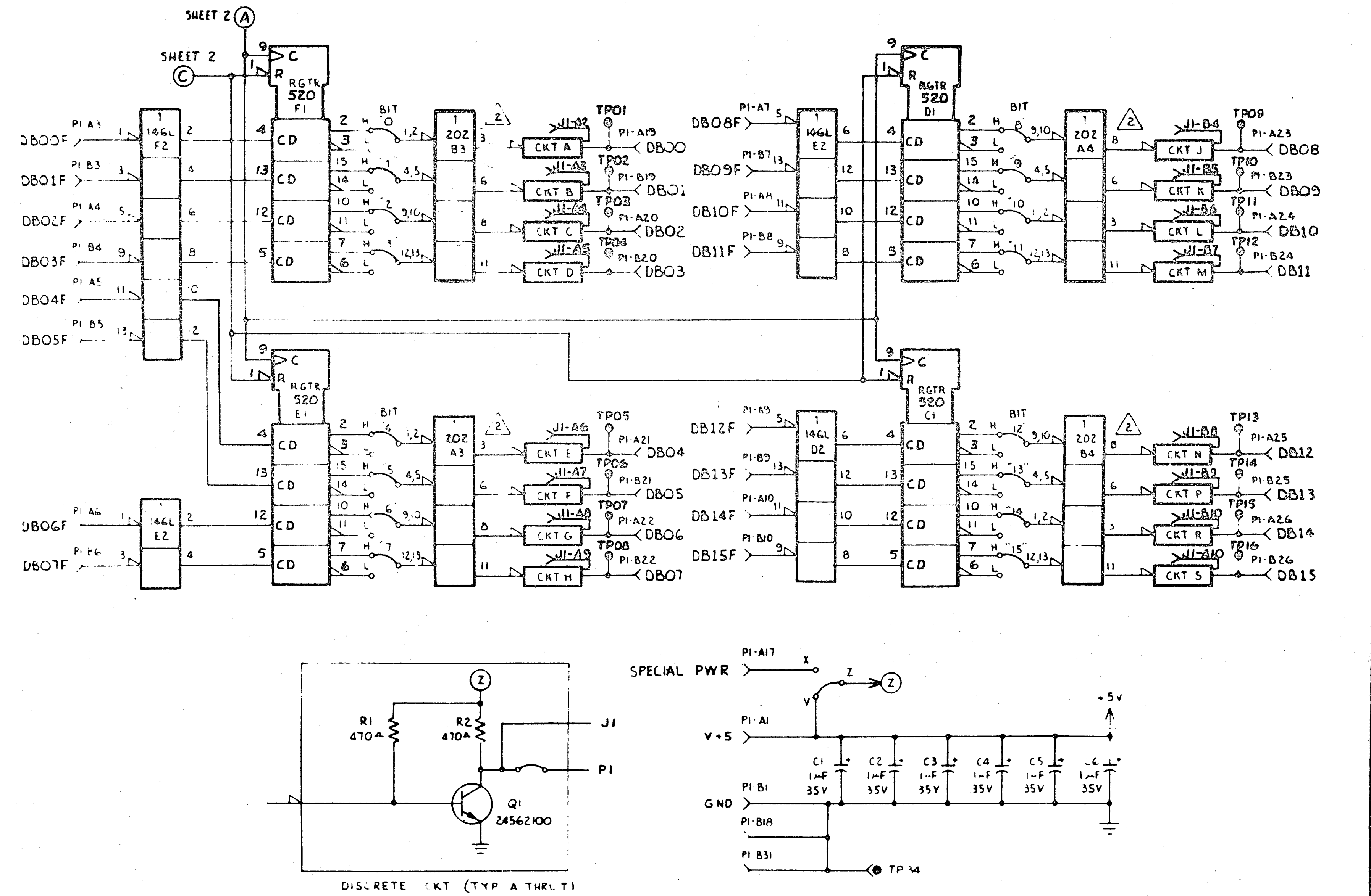
CARD POS

LOGIC TYPE 3SYT

C | CODE IDENT NO 09132 | DRAWING NUMBER

SHEET OF


MCLRF
PI-B13
WRITF
PI-B11
FUSTF
PI-A12
SSXXF
PI-A2
TP29
TP20
TP25
R1 3K
+5V
TP28
100ns
LOAD DATA 1-SHOT
SET READY 1-SHOT
TP27
SHEET 1
TP32
CONNECT
R7 20K
C9 50pF
R9 20K
READY
TP17
J1-B2
PI-B28
500 ns
+5V ENABLE READY 1-SHOT
R8 20K
C10 220pF
TP30
TP19
TP24
J1-B3
R3 75^
C7 470pF
RESET
INT/SYNC
TP18
PI-B2
FLXXF
PI-A28
CR1
CR2
MODE SELECTION
J2 ASYNC
J3 COMM
J4 SYNC
R4 1K
TP23
ENABLE REJECT 1-SHOT
R10 20K
TP26
REPLY
TP22
TP21
REJECT
PI-B12
RPLYF
PI-A13
RJCTF
J1-B1
PI-A29
REQST
CR3
CR4
R5 75^
C8 470pF
TP31
PI-B15
STALF
STALL
R6 3K
MCLR
SHEET 1
NOTES: UNLESS OTHERWISE SPECIFIED
CARD POS
LOGIC TYPE
3SYT
LOGIC DWG NO
88800200
REV
C
CODE IDENT NO.
09132
DRAWING NUMBER
SHEET 2
SHEET OF



4. P.W. BOARD HAS CAPABILITY TO ADD (2) CAPACITORS.

3. FOR KEY TO SYMBOLS SEE DWG 88981500.

2. ALL ELEMENT IDENTIFIER 202 & 203 ARE OPEN COLLECTOR.

1. ALL RESISTORS ARE 1/4 W.

NOTES UNLESS OTHERWISE SPECIFIED

DR 88800300 DETACHED LIST

	A	B	C	D	E	F
1			74175	74175	74175	74175
2				74L04	74L04	74L04
3	7403	7403				
4	7403	7403				
5						
6		7400	7414	7414	7403	74L04
7	840	840	74123	74123	9003	7405

LOGIC TITLE: DIGITAL OUTPUT UNIT – TRUE = +5V LL SYNC

LOGIC DWG NO 88800300 SH 1 OF 2 REV C

PWA NO 88800101 PWB NO 88800000

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION La Jolla Calif 92037

FIRST USED ON DA502

DR T. Cynamon 6-14-73

CHK B. Gilbert

ENGR [signature] 11 73

MFG

APPD [signature] 9/1/73

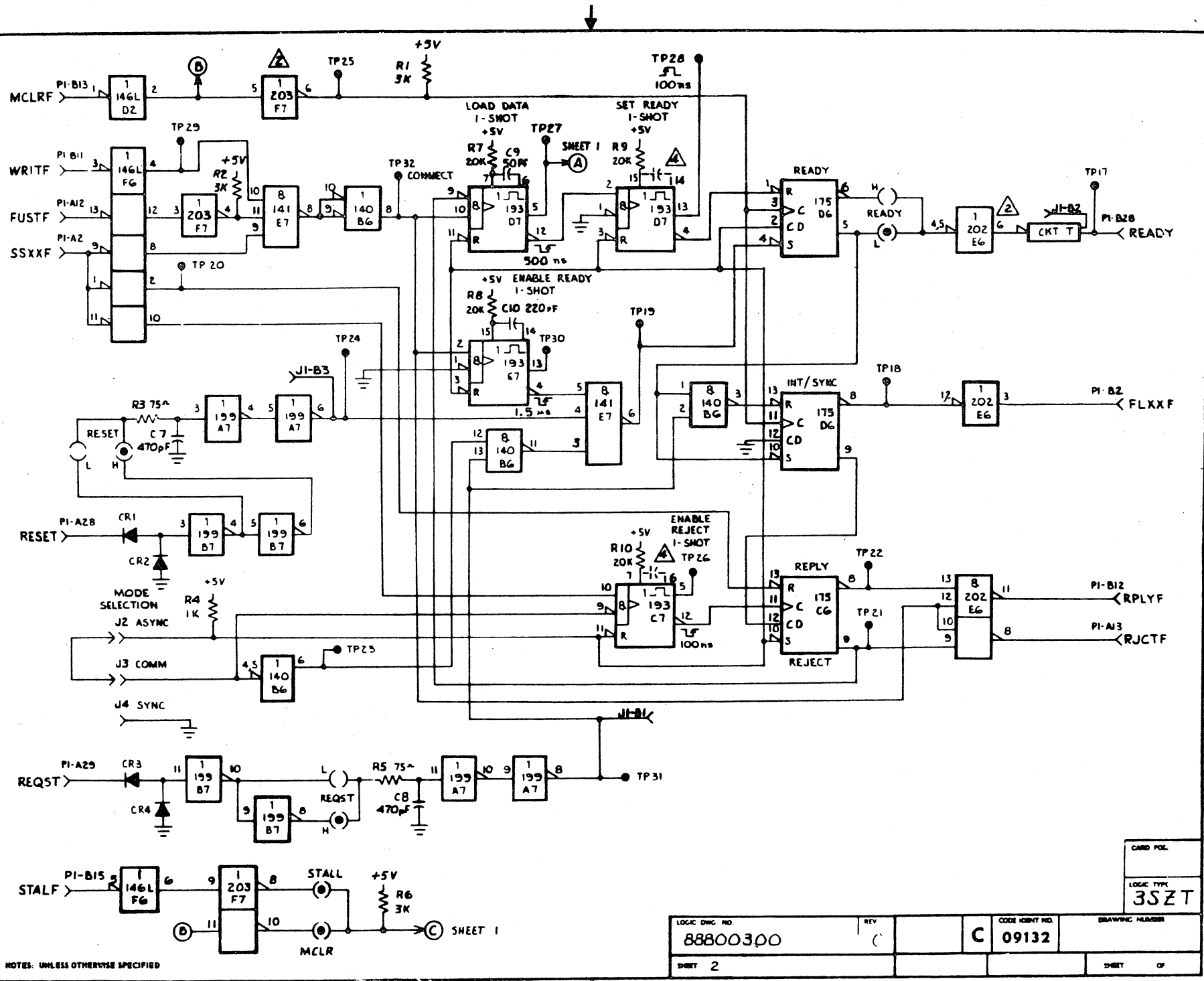
CARD POS

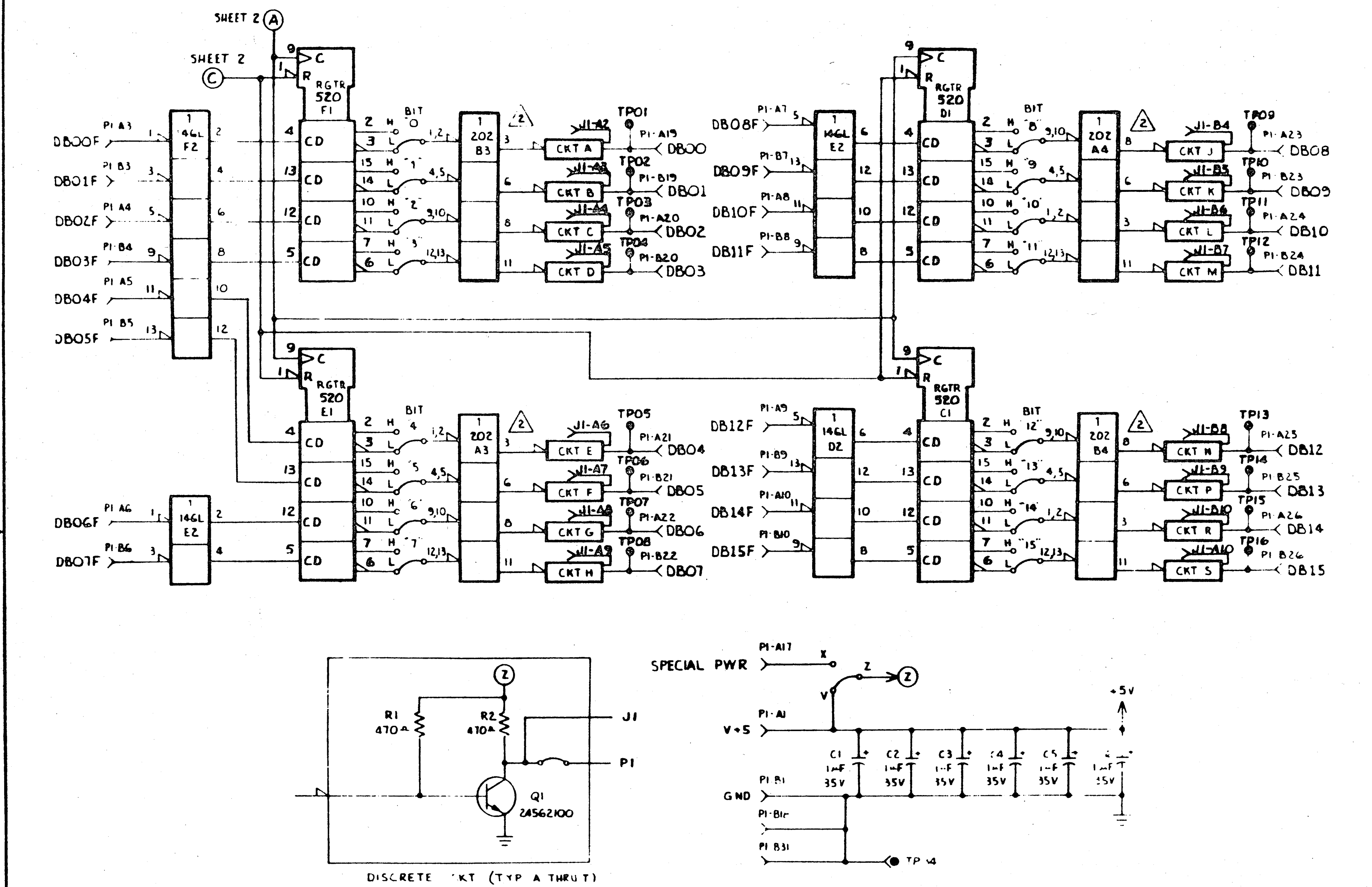
LOGIC TYPE 3SZT

C CODE IDENT NO 09132

DRAWING NUMBER

SHEET OF


MCLRF
P1-B13
WRITF
P1-B11
FUSTF
P1-A12
SSXXF
P1-A2
TP25
R1 3K
+5V
TP28
100ns
LOAD DATA 1-SHOT
SET READY 1-SHOT
TP29
TP27
SHEET 1
TP32 CONNECT
R7 20K
C9 50PF
R9 20K
R2 3K
READY
TP17
P1-B28
TP20
500 ns
+5V ENABLE READY 1-SHOT
R8 20K
C10 220PF
TP19
TP30
TP24
J1-B3
R3 75Ω
C7 470pF
RESET
1.5 μs
INT/SYNC
TP18
P1-B2
FLXXF
P1-A28
CR1
CR2
MODE SELECTION
J2 ASYNC
J3 COMM
J4 SYNC
R4 1K
ENABLE REJECT 1-SHOT
R10 20K
TP26
TP23
REPLY
TP22
TP21
REJECT
P1-B12
RPLYF
P1-A13
RJCTF
J1-B1
REQST
P1-A29
CR3
CR4
R5 75Ω
C8 470pF
TP31
STALF
P1-B15
STALL
R6 3K
MCLR
SHEET 1
NOTES: UNLESS OTHERWISE SPECIFIED
CARD POS.
LOGIC TYPE 3SZT
LOGIC DWG NO. 8880030
REV C
CODE IDENT NO. 09132
DRAWING NUMBER
SHEET 2
SHEET OF



4. F.W. BOARD HAS CAPABILITY TO ADD (2) CAPACITORS.

3. FOR KEY TO SYMBOLS SEE DWG 88931500

2. ALL ELEMENT IDENTIFIER 202 & 203 ARE OPEN COLLECTOR

1. ALL RESISTORS ARE 1/4 W.

NOTES UNLESS OTHERWISE SPECIFIED

DR 88800400 DETACHED LIST

	A	B	C	D	E	F
1			74175	74175	74175	74175
2				74L04	74L04	74L04
3	7403	7403				
4	7403	7403				
5						
6		7400	7414	7414	7403	74L04
7	840	840	74123	74123	9003	7405

LOGIC TITLE: DIGITAL OUTPUT UNIT – TRUE = 0v @ 65 MA, CC SYNC

LOGIC DWG NO: 88800400 SH 1 OF 2 — REV D

PWA NO: 88800102 — PWB NO: 88800000

CONTROL DATA — ANALOG DIGITAL SYSTEMS DIVISION, La Jolla Calif. 92037

FIRST USED ON: DA5C2

DR: T. [illegible] 6-14-73

CHK: [illegible]

ENGR: [illegible] 7-16-73

MFG:

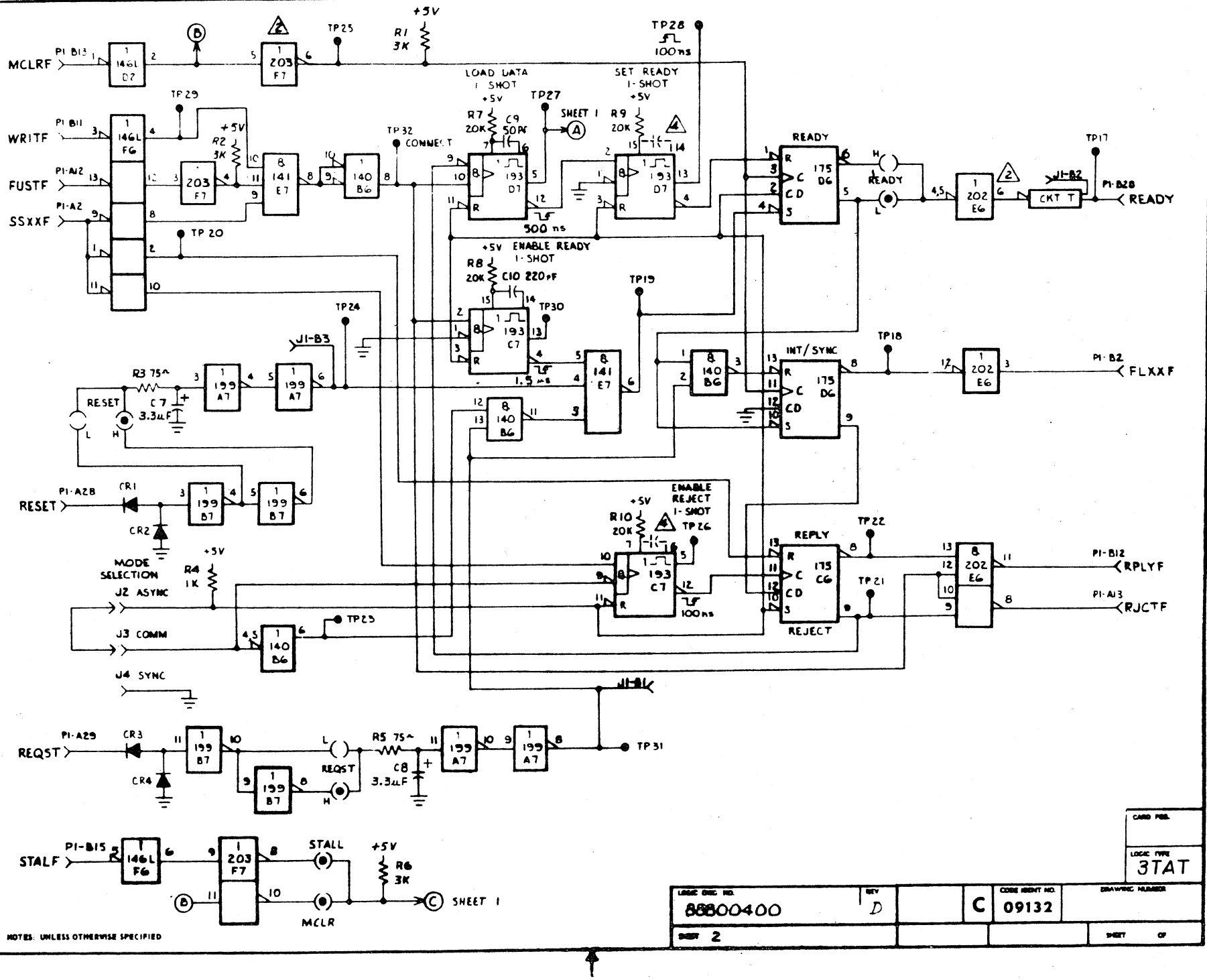
APPD: [illegible] Wall 1/7/73

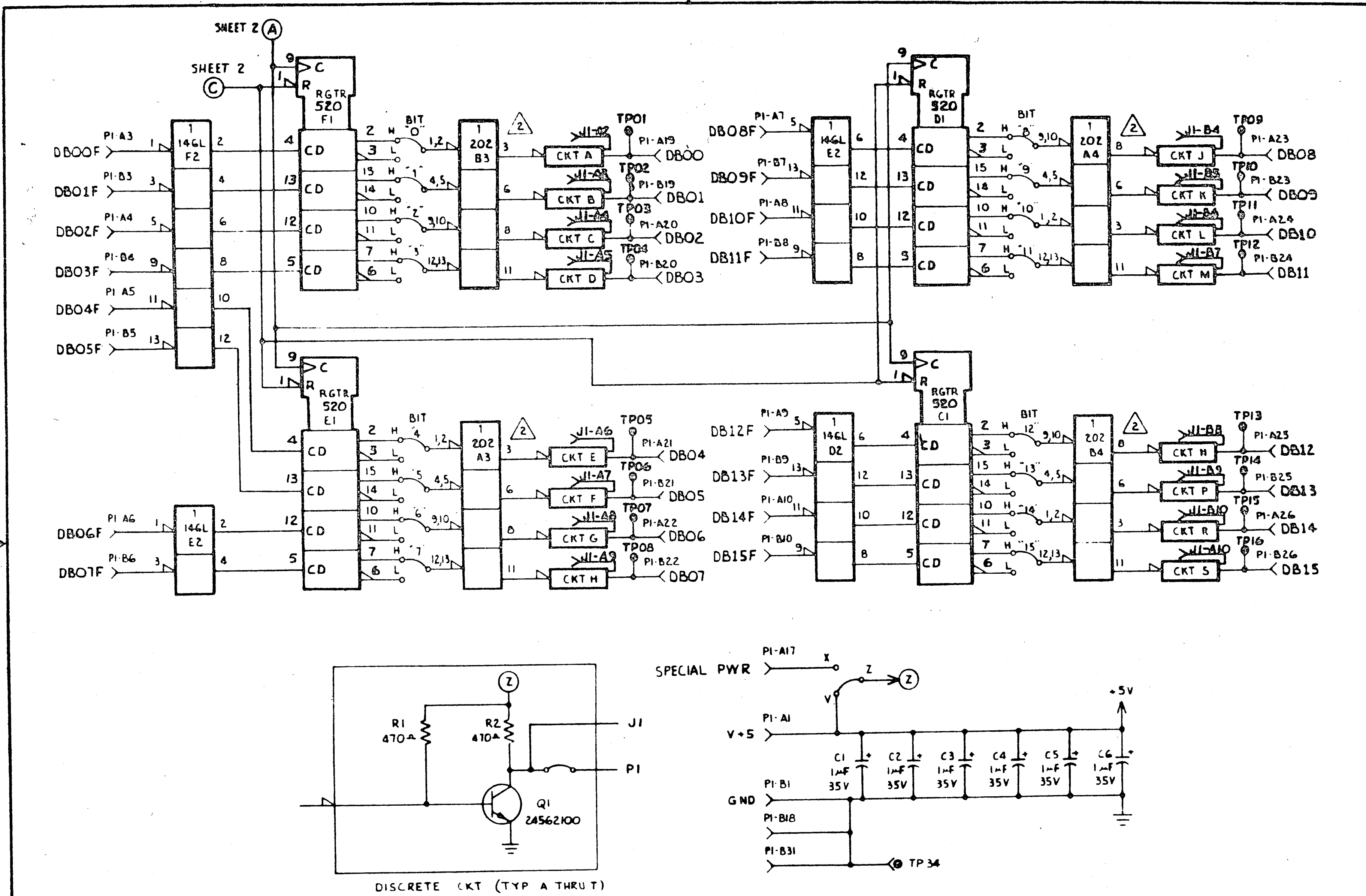
3TAT

CODE IDENT NO: C 09132

DRAWING NUMBER

SHEET OF


MCLRF
P1 B13
WRITF
P1 B11
FUSTF
P1-A12
SSXXF
P1-A2
RESET
P1-A28
REQST
P1-A29
STALF
P1-B15
+5V
R1 3K
TP25
TP28
100ns
LOAD DATA 1 SHOT
SET READY 1-SHOT
TP29
TP27
SHEET 1
TP32 CONNECT
R7 20K
C9 50PF
R9 20K
READY
TP17
P1-B28
R2 3K
ENABLE READY 1-SHOT
R8 20K
C10 220PF
TP30
TP19
TP24
J1-B3
R3 75^
C7 3.3μF
TP20
INT/SYNC
TP18
P1-B2
FLXXF
CR1
CR2
MODE SELECTION
J2 ASYNC
J3 COMM
J4 SYNC
R4 1K
ENABLE REJECT 1-SHOT
R10 20K
TP26
REPLY
TP22
TP21
REJECT
P1-B12
RPLYF
P1-A13
RJCTF
TP23
J1-B1
CR3
CR4
R5 75^
C8 3.3μF
TP31
STALL
R6 3K
MCLR
SHEET 1
1 146L D7
1 203 F7
1 146L F6
1 203 F7
8 141 E7
1 140 B6
8 140 B6
1 193 D7
1 193 C7
8 141 E7
8 140 B6
8 140 B6
1 199 A7
1 199 B7
1 175 DG
1 202 E6
CKT T
NOTES: UNLESS OTHERWISE SPECIFIED
CARD REQ.
LOGIC TYPE 3TAT
LOGIC DWG. NO. 88800400
REV D
C
CODE IDENT NO. 09132
DRAWING NUMBER
SHEET 2
SHEET OF



4. P.W. BOARD HAS CAPABILITY TO ADD (2) CAPACITORS.

3. FOR KEY TO SYMBOLS SEE DWG [illegible]

2. ALL ELEMENT IDENTIFIER 202 & 203 ARE OPEN COLLECTOR.

1. ALL RESISTORS ARE 1/4 W.

NOTES UNLESS OTHERWISE SPECIFIED

DR 88800500 — DETACHED LIST

	A	B	C	D	E	F
1			74175	74175	74175	74175
2				74L04	74L04	74L04
3	7403	7403				
4	7403	7403				
5						
6		7400	7474	7474	7409	74L04
7	840	840	74123	74123	9003	7405

LOGIC TITLE: DIGITAL OUTPUT UNIT – TRUE = +5V CC SYNC

LOGIC DWG NO: 88800500 SH 1 OF 2 — REV D

PWA NO: 88800103 — PWB NO: 88800000

CONTROL DATA — ANALOG-DIGITAL SYSTEMS DIVISION, La Jolla, Calif 92037

USED ON: DA502

DR: T. [illegible] 6-14-73

CHK: [signature] 7-25-73

ENGR: [signature] 7-26-73

MFG:

APPD: [signature] 9/7/73

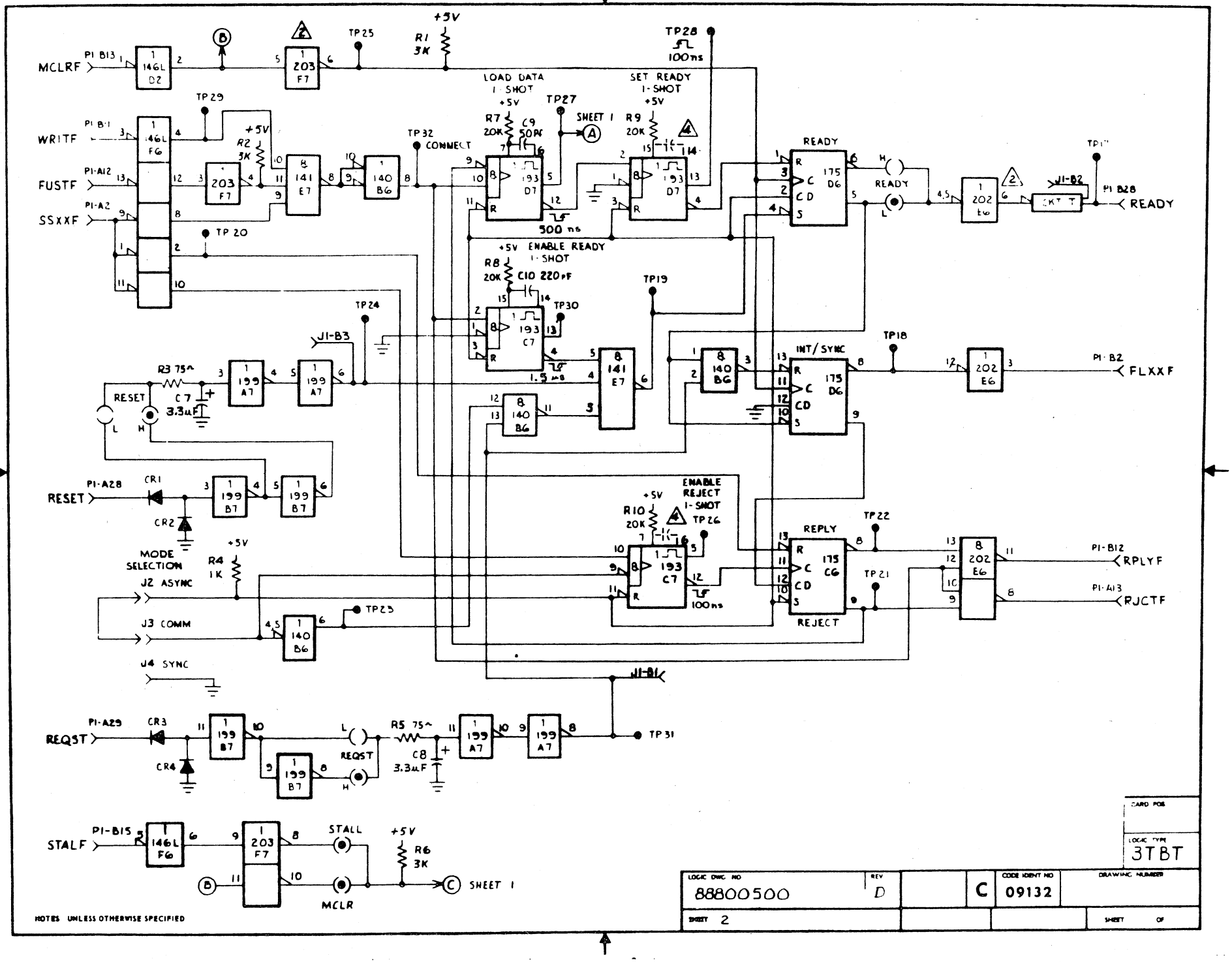
TITLE

CARD POS.

LOGIC TYPE: 3TBT

C — CODE IDENT NO. 09132 — DRAWING NUMBER

SHEET OF


MCLRF
P1 B13
WRITF
P1 B11
FUSTF
P1-A12
SSXXF
P1-A2
RESET
P1-A28
REQST
P1-A29
STALF
P1-B15
+5V
R1 3K
TP25
TP28
100ns
LOAD DATA 1-SHOT
SET READY 1-SHOT
TP29
TP27
SHEET 1
R7 20K
C9 50pF
R9 20K
TP32
CONNECT
R2 3K
500 ns
READY
P1 B28
TP20
ENABLE READY 1-SHOT
R8 20K
C10 220pF
TP30
TP19
TP24
J1-B3
1.5 μs
R3 75^
C7 3.3μF
INT/SYNC
TP18
P1-B2
FLXXF
CR1
CR2
MODE SELECTION
J2 ASYNC
J3 COMM
J4 SYNC
R4 1K
TP23
ENABLE REJECT 1-SHOT
R10 20K
TP26
REPLY
REJECT
TP22
TP21
P1-B12
RPLYF
P1-A13
RJCTF
J1-B1
CR3
CR4
REQST
R5 75^
C8 3.3μF
TP31
STALL
R6 3K
MCLR
SHEET 1
NOTES UNLESS OTHERWISE SPECIFIED
CARD POS
LOGIC TYPE
3TBT
LOGIC DWG NO
88800500
REV
D
C
CODE IDENT NO
09132
DRAWING NUMBER
SHEET 2
SHEET OF

Section Six

MAINTENANCE

6.1 PREVENTIVE MAINTENANCE

None required.

6.2 CALIBRATION AND ALIGNMENT

Not required.

6.3 TROUBLESHOOTING

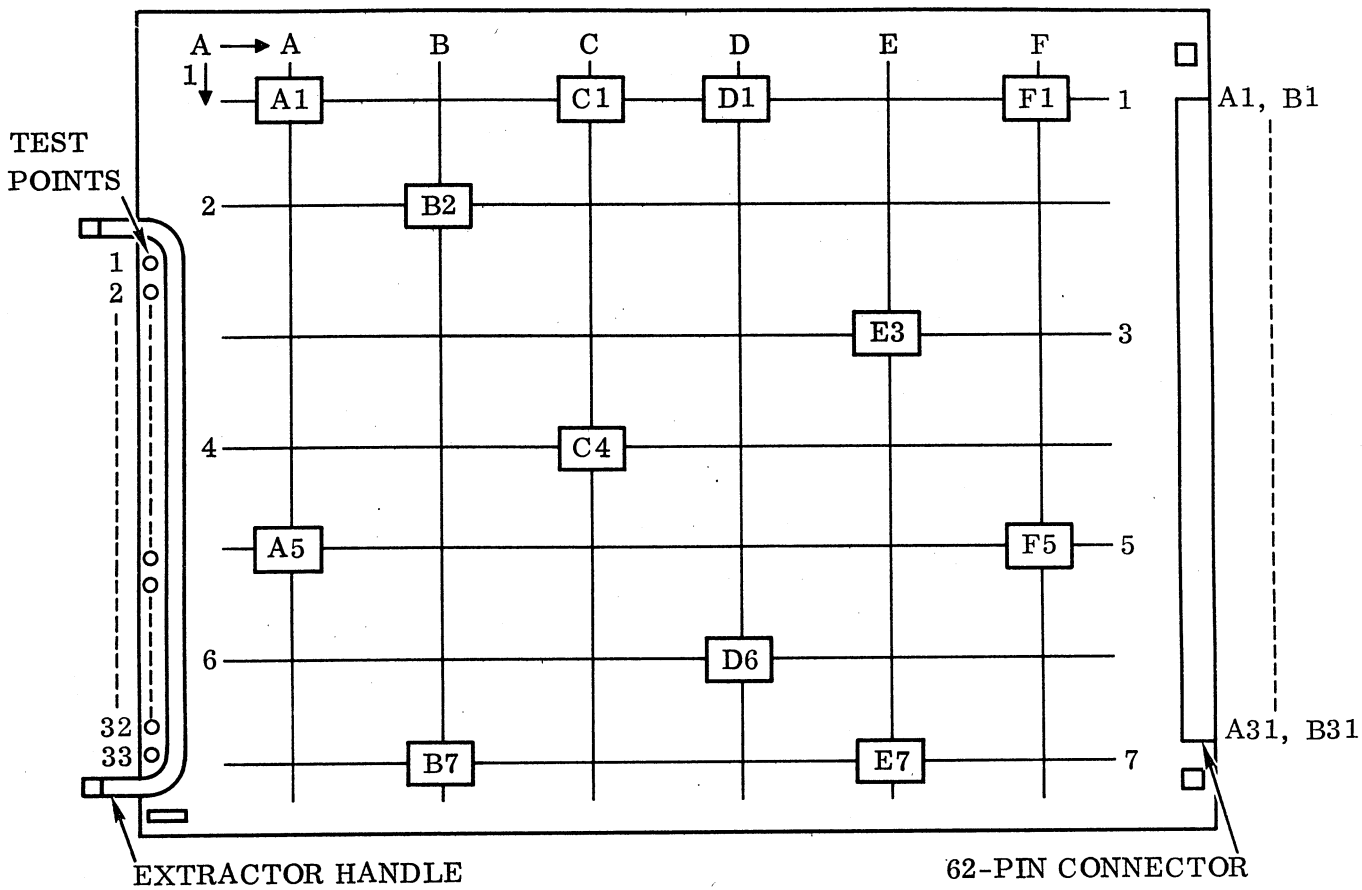
Troubleshooting can be performed on the DOU (when controlled by a 1700/1770 computer) by using Section 9 of Test 90, SMM17 diagnostic. Refer to the SMM17 Reference Manual. Section 11 can be performed when a digital input unit (DIU) is connected to the DOU. Error printouts are provided specifying the instruction performed, expected and actual results, and the condition causing the error.

The DOU can be interchanged with a like version for troubleshooting when the jumpers for mode, request, reset, and ready signals are properly positioned.

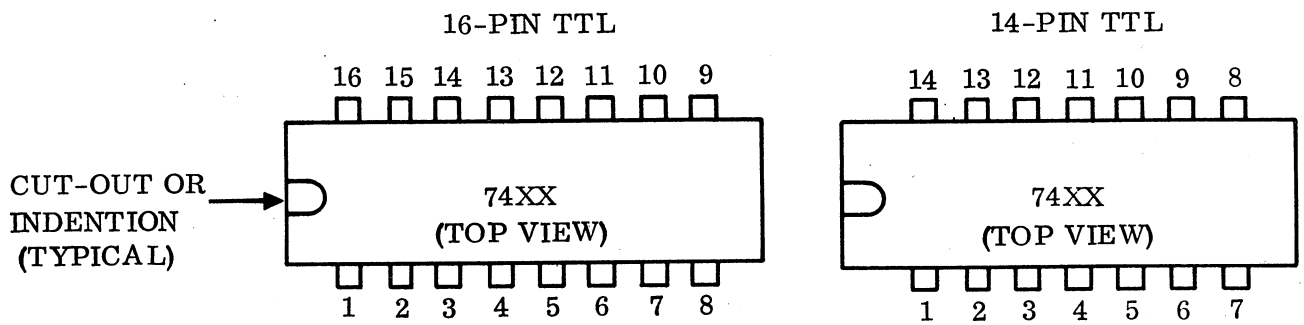
6.4 MAINTENANCE AIDS

Use the following as maintenance aids:

- Card extender, 9-inch logic type, 2NMT Card No. 39844100.
- Digital Input Unit (DIU), Part No. 39842200.
- Standard pin and chip locations (see Figure 6.1).
- Integrated circuit logic symbols are shown in the Key to Logic Symbols Manual.



PRINTED WIRING BOARD (PWB) COMPONENT SIDE CHIP LOCATION



PIN CONFIGURATION, TOP VIEW

Figure 6.1. Board Component and Pin Location

Section Seven

PARTS DATA

7.1 PARTS DATA

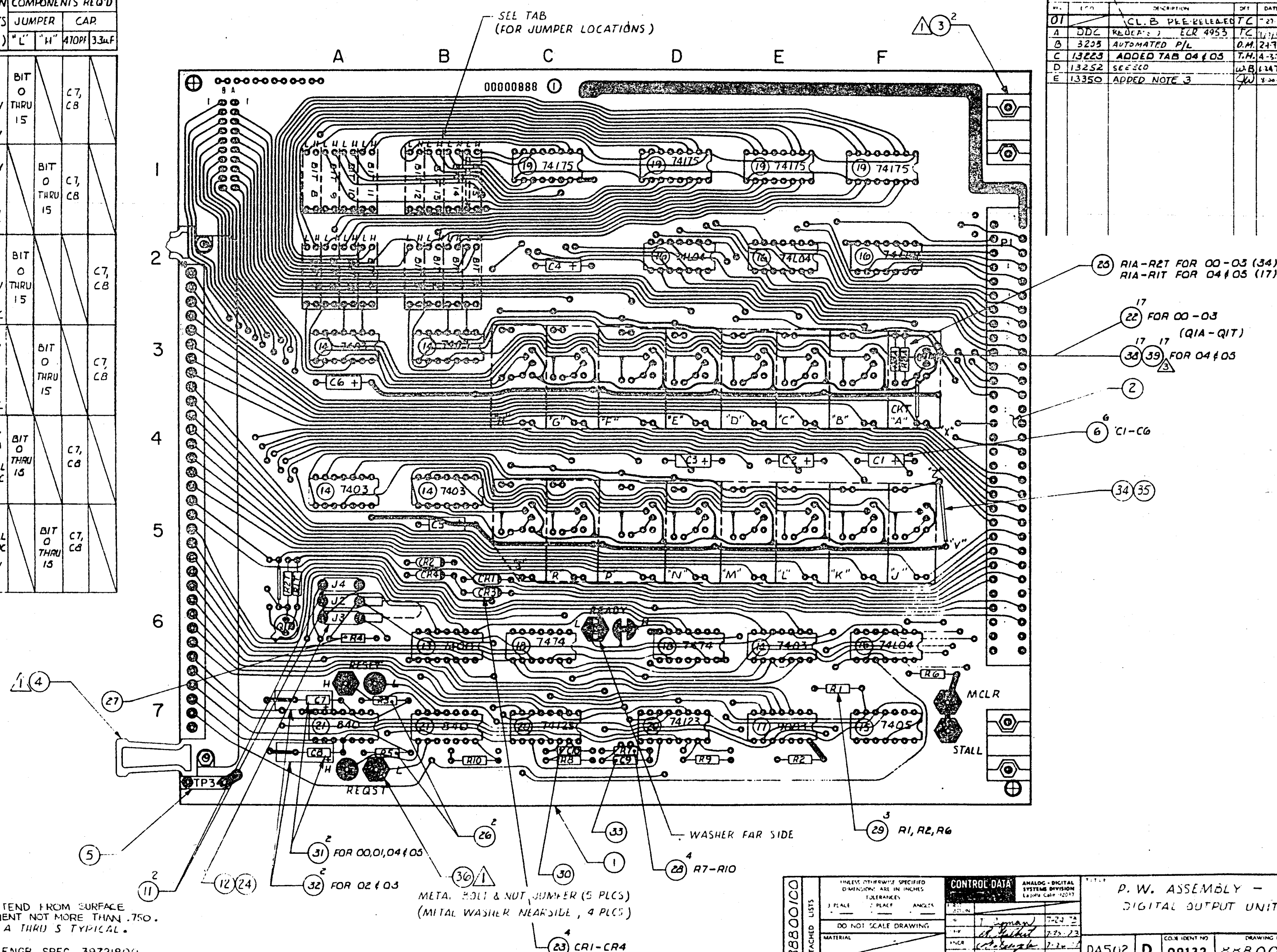
This section contains the printed wiring assembly and parts lists for the digital output unit (DOU).

00100888

PART NO.	EQUIP NO.	LOGIC TYPE	LOGIC NO	FUNCTION (16 OUTPUTS & SYNC)	COMPONENTS REQ'D JUMPER "L"	JUMPER "H"	CAP. 470PF	CAP. 3.3uF
88800100	DA502E	3SYT	88800200	LL, TRUE=0V @ 65 MA FALSE=+5V SYNC SIG (LL) 0 +5V	BIT 0 THRU 15		C7, C8	
88800101	DA502F	3SZT	88800300	LL, TRUE=+5V FALSE=0V @ 65 MA SYNC SIG (LL) 0, +5V		BIT 0 THRU 15	C7, C8	
88800102	DA502G	3TAT	88800400	LL, TRUE=0V @ 65 MA FALSE=+5V SYNC SIG (CC) FORM C	BIT 0 THRU 15			C7, C8
88800103	DA502H	3TBT	88800500	LL, TRUE=+5V FALSE=0V @ 65 MA SYNC SIG (CC) FORM C		BIT 0 THRU 15		C7, C8
88800104	DA502J	4UYT	88766000	LL, TRUE=0V @ 125 MA FALSE= OPEN COLL TO +28VDC	BIT 0 THRU 15		C7, C8	
88800105	DA502K	4UZT	88766300	LL, TRUE= OPEN COLL TO +28VDC FALSE=0V @ 125 MA		BIT 0 THRU 15	C7, C8	

REVISION RECORD

LTR	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
01		CL. B PRE-RELEASED	TC			
A	DDC	RELEASED ECR 4953	TC			
B	3235	AUTOMATED P/L	D.M.	2-4-74	BR	
C	13223	ADDED TAB 04 & 05	T.H.	4-3-74		
D	13252	SEE ECO	W.B.			
E	13350	ADDED NOTE 3				



3. COMPONENT HEIGHT MAY EXTEND FROM SURFACE OF BOARD TO TOP OF COMPONENT NOT MORE THAN .750.
2. CKTS A & T SHOWN. CKTS A THRU S TYPICAL.
1. TO BE ASSEMBLED TO CDC ENGR SPEC 39721800

NOTES: UNLESS OTHERWISE SPECIFIED

PL 88800100 DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES
DO NOT SCALE DRAWING

CONTROL DATA — ANALOG-DIGITAL SYSTEMS DIVISION

P. W. ASSEMBLY - DIGITAL OUTPUT UNIT

DA502 | D | 09132 | 88800100

SCALE 2/1 — SHEET 1 OF 1

DWN	T. Cuman	6-6-73
CHKD	R. Gilbert	7-23-73
ENG	R W Taylor	7-26-73
MFG		
APPR	D E Wall	9/7/73

CONTROL DATA

ANALOG - DIGITAL SYSTEMS DIVISION
La Jolla, Calif. 92037

CODE IDENT 09132

TITLE: PW ASSY — DIGITAL OUTPUT UNIT

FIRST USED ON

PREFIX	DOCUMENT NO.	REV
PL	88800100	E

DA502

SHEET 1 OF 9

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	
01		CL.B PRE-RELEASED	TC	7-27-73	
A	DDC	RELEASED ECR 4953	TC	9/7/73	
B	13205	PUT P/L ON COMMAND	O.M.	2-1-74	
C	13229	ADDED TAB 04 & 05	T.H.	4-3-74	
D	13252	SEE ECO	WJB	6-24-74	
E	13350	DWG CHG ONLY		8-20-74	

NOTES:

DETACHED LISTS

AA3188

PRINTED IN U.S.A.

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CLASSIFICATION NUMBER
88800100	E	CLA	D	PWA-DIG OUT,TRUE=0V LL (3SYT)	DS	IOM	01/29/74	

MF

PROCESSING DATE	PAGE NUMB
07/30/74	~~1~~

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD NUMBER	DATE EFFECTIVE	CLASSIFICATION NUMBER	OP NUMBER	MAKE/BUY PART TYPE	PN NC	S OR N
14	A	15104200	500	PC	IC QUAD 2IN NAND GATE 7403	IN					PPP4		N
19	A	15104500	400	PC	ACCEPT TEST TYPE 74175	IN					PPP4		N
18	A	15104800	200	PC	IC SPEC DUAL D TYPE FF 7474	IN					PPP4		N
16	B	15112700	400	PC	INT CKT 74L04	IN							N
21	B	15112800	200	PC	MICRO CKT DTL HEX INVERTER	IN					PPP4		N
15	A	17184600	100	PC	HEX INVERT 14 PIN DUAL-IN-LINE	IN					PPP4		N
26	C	24500036	200	PC	RES FXD .25W 75 OHMS	IN					PPP4		N
25	C	24500055	3400	PC	RES FXD .25W 470 OHMS	IN					PPP4		N
27	C	24500063	100	PC	RES FXD .25W 1000 OHMS	IN					PPP4		N
29	C	24500074	300	PC	RES FXD .25W 3000 OHMS	IN					PPP4		N
28	C	24500094	400	PC	RES FXD .25W 20000 OHMS	IN					PPP4		N
34	C	24501806	100	IN	WIRE ELECT SOLID COPPER 24 GA	IN					PPP1		N
6	C	24505229	600	PC	CAP. FXD TANT 1 MF 35 VOLT	IN					PPP4		N
22	C	24562100	1700	PC	TSTR SILICON-PLANAR,NPN	IN					PPP4		N
23	A	25175800	400	PC	DIODE(1N914)	IN							N
37	B	38933500	100	PC	LABEL,IDENTIFICATION	IN							N
5	A	38958502	100	PC	TEST JACK, BLACK	IN							N
11	A	38958507	200	PC	TEST JACK, YELLOW	IN							N
12	A	38958509	100	PC	TEST JACK, PURPLE	IN							N
24	B	38991203	100	PC	PATCHCORD 1 IN. LG.	IN							N
35	A	39181003	100	IN	INSULATION, TEFLON, 24 AWG	IN	013256						N
13	B	39388300	100	PC	INT CKT 7400	IN							N
20	B	39389800	200	PC	INT CKT 74123	IN							N
36	A	39721800	REF	PC	ASSEMBLY REQUIREMENT	IN							N
3	C	39827500	200	PC	GUIDE,APPROACH	IN							N
17	A	50250700	100	PC	I.C. TTL TRIPPLE 3 INPUT NAND	IN					PPP4		N
4	D	52936000	100	PC	AIR SEAL - 25 PAK	IN					PPP4		N
33	A	84996708	100	PC	CAP, CER, 50 PF	IN							N
30	A	84996717	100	PC	CAP, CER, 220 PF	IN							N
31	A	84996721	200	PC	CAP, CER, 470 PF	IN							N
1	C	88800000	100	PC	PWB DIGITAL OUTPUT	IN							N
7	C	88800200	REF	PC	LOGIC DIAGRAM (3SYT)	IN							N
2	C	94243400	100	PC	CONNECTOR-CARD MTG 62 SOCKET	IN					PPP4		N
					NUMBER OF LINE ITEMS = 33								
					HIGHEST FIND NUMBER = 37								

PROJECT ENGINEER
R. DENGLER

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CLASSIFICATION NUMBER
88800101	E	CLA	D	PWA-DIG OUT TRUE=+5V LL (3SZT)	DS	IOM	01/29/74	

MF

PROCESSING DATE	PAGE NUMBER
07/30/74	~~1~~ 1

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	CLASSIFICATION NUMBER	OP NUMBER	MAKE/BUY PART TYPE	PN NC	S OR N
14	A	15104200	500	PC	IC QUAD 2IN NAND GATE 7403	IN					PPP4		N
19	A	15104500	400	PC	ACCEPT TEST TYPE 74175	IN					PPP4		N
18	A	15104800	200	PC	IC SPEC DUAL D TYPE FF 7474	IN					PPP4		N
16	B	15112700	400	PC	INT CKT 74L04	IN							N
21	B	15112800	200	PC	MICRO CKT DTL HEX INVERTER	IN					PPP4		N
15	A	17184600	100	PC	HEX INVERT 14 PIN DUAL-IN-LINE	IN					PPP4		N
26	C	24500036	200	PC	RES FXD .25W 75 OHMS	IN					PPP4		N
25	C	24500055	3400	PC	RES FXD .25W 470 OHMS	IN					PPP4		N
27	C	24500063	100	PC	RES FXD .25W 1000 OHMS	IN					PPP4		N
29	C	24500074	300	PC	RES FXD .25W 3000 OHMS	IN					PPP4		N
28	C	24500094	400	PC	RES FXD .25W 20000 OHMS	IN					PPP4		N
34	C	24501806	100	IN	WIRE ELECT SOLID COPPER 24 GA	IN					PPP1		N
6	C	24505229	600	PC	CAP. FXD TANT 1 MF 35 VOLT	IN					PPP4		N
22	C	24562100	1700	PC	TSTR SILICON-PLANAR,NPN	IN					PPP4		N
23	A	25175800	400	PC	DIODE(1N914)	IN							N
37	B	38933500	100	PC	LABEL,IDENTIFICATION	IN							N
5	A	38958502	100	PC	TEST JACK, BLACK	IN							N
11	A	38958507	200	PC	TEST JACK, YELLOW	IN							N
12	A	38958509	100	PC	TEST JACK, PURPLE	IN							N
24	B	38991203	100	PC	PATCHCORD 1 IN. LG.	IN							N
35	A	39181003	100	IN	INSULATION, TEFLON, 24 AWG	IN	013256						N
13	B	39388300	100	PC	INT CKT 7400	IN							N
20	B	39389800	200	PC	INT CKT 74123	IN							N
36	A	39721800	REF	PC	ASSEMBLY REQUIREMENT	IN							N
3	C	39827500	200	PC	GUIDE,APPROACH	IN							N
17	A	50250700	100	PC	I.C. TTL TRIPPLE 3 INPUT NAND	IN					PPP4		N
4	D	52936000	100	PC	AIR SEAL - 25 PAK	IN					PPP4		N
33	A	84996708	100	PC	CAP, CER, 50 PF	IN							N
30	A	84996717	100	PC	CAP, CER, 220 PF	IN							N
31	A	84996721	200	PC	CAP, CER, 470 PF	IN							N
1	C	88800000	100	PC	PWB DIGITAL OUTPUT	IN							N
8	C	88800300	REF	PC	LOGIC DIAGRAM (3SZT)	IN							N
2	C	94243400	100	PC	CONNECTOR-CARD MTG 62 SOCKET	IN					PPP4		N
					NUMBER OF LINE ITEMS = 33								
					HIGHEST FIND NUMBER = 37								

PROJECT ENGINEER
R. DENGLER

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RECYCLE FOR THE FUTURE

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CLASSIFICATION NUMBER
88800102	E	CLA	D	PWA-DIG OUT TRUE=0V CC (3TAT)	DS	IOM	01/29/74	

MF

PROCESSING DATE	PAGE NUMBER
07/30/74	1

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD NUMBER	DATE EFFECTIVE	CLASSIFICATION NUMBER	OP NUMBER	MAKE/BUY PART TYPE	PN NC	S OR N
14	A	15104200	500	PC	IC QUAD 2IN NAND GATE 7403	IN					PPP4		N
19	A	15104500	400	PC	ACCEPT TEST TYPE 74175	IN					PPP4		N
18	A	15104800	200	PC	IC SPEC DUAL D TYPE FF 7474	IN					PPP4		N
16	B	15112700	400	PC	INT CKT 74L04	IN							N
21	B	15112800	200	PC	MICRO CKT DTL HEX INVERTER	IN					PPP4		N
15	A	17184600	100	PC	HEX INVERT 14 PIN DUAL-IN-LINE	IN					PPP4		N
26	C	24500036	200	PC	RES FXD .25W 75 OHMS	IN					PPP4		N
25	C	24500055	3400	PC	RES FXD .25W 470 OHMS	IN					PPP4		N
27	C	24500063	100	PC	RES FXD .25W 1000 OHMS	IN					PPP4		N
29	C	24500074	300	PC	RES FXD .25W 3000 OHMS	IN					PPP4		N
28	C	24500094	400	PC	RES FXD .25W 20000 OHMS	IN					PPP4		N
34	C	24501806	100	IN	WIRE ELECT SOLID COPPER 24 GA	IN					PPP1		N
6	C	24505229	600	PC	CAP. FXD TANT 1 MF 35 VOLT	IN					PPP4		N
32	C	24505235	200	PC	CAPACITOR FIXED 10 PCT 3.3 MF	IN					PPP4		N
22	C	24562100	1700	PC	TSTR SILICON-PLANAR,NPN	IN					PPP4		N
23	A	25175800	400	PC	DIODE(1N914)	IN							N
37	B	38933500	100	PC	LABEL,IDENTIFICATION	IN							N
5	A	38958502	100	PC	TEST JACK, BLACK	IN							N
11	A	38958507	200	PC	TEST JACK, YELLOW	IN							N
12	A	38958509	100	PC	TEST JACK, PURPLE	IN							N
24	B	38991203	100	PC	PATCHCORD 1 IN. LG.	IN							N
35	A	39181003	100	IN	INSULATION, TEFLON, 24 AWG	IN	013256						N
13	B	39388300	100	PC	INT CKT 7400	IN							N
20	B	39389800	200	PC	INT CKT 74123	IN							N
36	A	39721800	REF	PC	ASSEMBLY REQUIREMENT	IN							N
3	C	39827500	200	PC	GUIDE,APPROACH	IN							N
17	A	50250700	100	PC	I.C. TTL TRIPPLE 3 INPUT NAND	IN					PPP4		N
4	D	52936000	100	PC	AIR SEAL - 25 PAK	IN					PPP4		N
33	A	84996708	100	PC	CAP, CER, 50 PF	IN							N
30	A	84996717	100	PC	CAP, CER, 220 PF	IN							N
1	C	88800000	100	PC	PWB DIGITAL OUTPUT	IN							N
9	C	88800400	REF	PC	LOGIC DIAGRAM (3TAT)	IN							N
2	C	94243400	100	PC	CONNECTOR-CARD MTG 62 SOCKET	IN					PPP4		N
					NUMBER OF LINE ITEMS = 33								
					HIGHEST FIND NUMBER = 37								

PROJECT ENGINEER
R. DENGLER

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CLASSIFICATION NUMBER
88800103	E	CLA	D	PWA-DIG OUT TRUE=+5V CC (3TBT)	DS	IOM	01/29/74	

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PROCESSING DATE	PAGE NUMBER
07/30/74	~~1~~ 1

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD NUMBER	DATE EFFECTIVE	CLASSIFICATION NUMBER	OP NUMBER	MAKE/BUY PART TYPE	PN NC	S OR N
14	A	15104200	500	PC	IC QUAD 2IN NAND GATE 7403	IN					PPP4		N
19	A	15104500	400	PC	ACCEPT TEST TYPE 74175	IN					PPP4		N
18	A	15104800	200	PC	IC SPEC DUAL D TYPE FF 7474	IN					PPP4		N
16	B	15112700	400	PC	INT CKT 74L04	IN							N
21	B	15112800	200	PC	MICRO CKT DTL HEX INVERTER	IN					PPP4		N
15	A	17184600	100	PC	HEX INVERT 14 PIN DUAL-IN-LINE	IN					PPP4		N
26	C	24500036	200	PC	RES FXD .25W 75 OHMS	IN					PPP4		N
25	C	24500055	3400	PC	RES FXD .25W 470 OHMS	IN					PPP4		N
27	C	24500063	100	PC	RES FXD .25W 1000 OHMS	IN					PPP4		N
29	C	24500074	300	PC	RES FXD .25W 3000 OHMS	IN					PPP4		N
28	C	24500094	400	PC	RES FXD .25W 20000 OHMS	IN					PPP4		N
34	C	24501806	100	IN	WIRE ELECT SOLID COPPER 24 GA	IN					PPP1		N
6	C	24505229	600	PC	CAP. FXD TANT 1 MF 35 VOLT	IN					PPP4		N
32	C	24505235	200	PC	CAPACITOR FIXED 10 PCT 3.3 MF	IN					PPP4		N
22	C	24562100	1700	PC	TSTR SILICON-PLANAR,NPN	IN					PPP4		N
23	A	25175800	400	PC	DIODE(1N914)	IN							N
37	B	38933500	100	PC	LABEL,IDENTIFICATION	IN							N
5	A	38958502	100	PC	TEST JACK, BLACK	IN							N
11	A	38958507	200	PC	TEST JACK, YELLOW	IN							N
12	A	38958509	100	PC	TEST JACK, PURPLE	IN							N
24	B	38991203	100	PC	PATCHCORD 1 IN. LG.	IN							N
35	A	39181003	100	IN	INSULATION, TEFLON, 24 AWG	IN	013256						N
13	B	39388300	100	PC	INT CKT 7400	IN							N
20	B	39389800	200	PC	INT CKT 74123	IN							N
36	A	39721800	REF	PC	ASSEMBLY REQUIREMENT	IN							N
3	C	39827500	200	PC	GUIDE,APPROACH	IN							N
17	A	50250700	100	PC	I.C. TTL TRIPPLE 3 INPUT NAND	IN					PPP4		N
4	D	52936000	100	PC	AIR SEAL - 25 PAK	IN					PPP4		N
33	A	84996708	100	PC	CAP, CER, 50 PF	IN							N
30	A	84996717	100	PC	CAP, CER, 220 PF	IN							N
1	C	88800000	100	PC	PWB DIGITAL OUTPUT	IN							N
10	C	88800500	REF	PC	LOGIC DIAGRAM (3TBT)	IN							N
2	C	94243400	100	PC	CONNECTOR-CARD MTG 62 SOCKET	IN					PPP4		N
					NUMBER OF LINE ITEMS = 33								
					HIGHEST FIND NUMBER = 37								

PROJECT ENGINEER
R. DENGLER

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RECYCLE FOR THE FUTURE

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CLASSIFICATION NUMBER		PROCESSING DATE	PAGE NUMBER
88800104	E	CLA	D	PWA-DIG OUT TRUE=0V LL (4UYT)	DS	IOM	04/12/74		MF	07/30/74	~~1~~ 2

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	CLASSIFICATION NUMBER	OP NUMBER	MAKE/BUY PART TYPE	PN NC	S OR N
14	A	15104200	500	PC	IC QUAD 2IN NAND GATE 7403	IN					PPP4		N
19	A	15104500	400	PC	ACCEPT TEST TYPE 74175	IN					PPP4		N
18	A	15104800	200	PC	IC SPEC DUAL D TYPE FF 7474	IN					PPP4		N
16	B	15112700	400	PC	INT CKT 74L04	IN							N
21	B	15112800	200	PC	MICRO CKT DTL HEX INVERTER	IN					PPP4		N
15	A	17184600	100	PC	HEX INVERT 14 PIN DUAL-IN-LINE	IN					PPP4		N
26	C	24500036	200	PC	RES FXD .25W 75 OHMS	IN					PPP4		N
25	C	24500055	1700	PC	RES FXD .25W 470 OHMS	IN					PPP4		N
27	C	24500063	100	PC	RES FXD .25W 1000 OHMS	IN					PPP4		N
29	C	24500074	300	PC	RES FXD .25W 3000 OHMS	IN					PPP4		N
28	C	24500094	400	PC	RES FXD .25W 20000 OHMS	IN					PPP4		N
34	C	24501806	100	IN	WIRE ELECT SOLID COPPER 24 GA	IN					PPP1		N
6	C	24505229	600	PC	CAP. FXD TANT 1 MF 35 VOLT	IN					PPP4		N
23	A	25175800	400	PC	DIODE(1N914)	IN							N
38	C	36143500	1700	PC	TRANSISTOR 2N3642	OUT	013252	041974			PPP4		N
37	B	38933500	100	PC	LABEL,IDENTIFICATION	IN							N
5	A	38958502	100	PC	TEST JACK, BLACK	IN							N
11	A	38958507	200	PC	TEST JACK, YELLOW	IN							N
12	A	38958509	100	PC	TEST JACK, PURPLE	IN							N
24	B	38991203	100	PC	PATCHCORD 1 IN. LG.	IN							N
35	A	39181003	100	IN	INSULATION, TEFLON, 24 AWG	IN	013256						N
13	B	39388300	100	PC	INT CKT 7400	IN							N
20	B	39389800	200	PC	INT CKT 74123	IN							N
36	A	39721800	REF	PC	ASSEMBLY REQUIREMENT	IN							N
3	C	39827500	200	PC	GUIDE,APPROACH	IN							N
38	A	50210500	1700	PC	TRANSISTOR 2N3642	IN	013252	041974					N
17	A	50250700	100	PC	I.C. TTL TRIPPLE 3 INPUT NAND	IN					PPP4		N
4	D	52936000	100	PC	AIR SEAL - 25 PAK	IN					PPP4		N
39	A	84905500	1700	PC	MTG PAD,TRANSISTOR	IN							N
33	A	84996708	100	PC	CAP, CER, 50 PF	IN							N
30	A	84996717	100	PC	CAP, CER, 220 PF	IN							N
31	A	84996721	200	PC	CAP, CER, 470 PF	IN							N
40	C	88788000	REF	PC	LOGIC DIAGRAM (4UYT)	IN							N
1	C	88800000	100	PC	PWB DIGITAL OUTPUT	IN							N
2	C	94243400	100	PC	CONNECTOR-CARD MTG 62 SOCKET	IN					PPP4		N
					NUMBER OF LINE ITEMS = 35								

PROJECT ENGINEER
R. DENGLER

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CLASSIFICATION NUMBER		PROCESSING DATE	PAGE NUMBER
88800104	E	CLA	D	PWA-DIG OUT TRUE=0V LL (4UYT)	DS	IOM	04/12/74		MF	07/30/74	~~2~~ 2

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD NUMBER	DATE EFFECTIVE	CLASSIFICATION NUMBER	OP NUMBER	MAKE/BUY PART TYPE	PN NC	S OR N

HIGHEST FIND NUMBER = 40

R. DENGLER

PROJECT ENGINEER

RECYCLE FOR THE FUTURE

AA 2709 REV. 2-73

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CLASSIFICATION NUMBER		PROCESSING DATE	PAGE NUMBER
88800105	E	CLA	D	PWA-DIG OUT TRUE=+28V LL(4UZT)	DS	IOM	04/12/74		MF	07/30/74	~~1~~ 2

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	CLASSIFICATION NUMBER	OP NUMBER	MAKE/BUY PART TYPE	PN NC	S OR N
14	A	15104200	500	PC	IC QUAD 2IN NAND GATE 7403	IN					PPP4		N
19	A	15104500	400	PC	ACCEPT TEST TYPE 74175	IN					PPP4		N
18	A	15104800	200	PC	IC SPEC DUAL D TYPE FF 7474	IN					PPP4		N
16	B	15112700	400	PC	INT CKT 74L04	IN							N
21	B	15112800	200	PC	MICRO CKT DTL HEX INVERTER	IN					PPP4		N
15	A	17184600	100	PC	HEX INVERT 14 PIN DUAL-IN-LINE	IN					PPP4		N
26	C	24500036	200	PC	RES FXD .25W 75 OHMS	IN					PPP4		N
25	C	24500055	1700	PC	RES FXD .25W 470 OHMS	IN					PPP4		N
27	C	24500063	100	PC	RES FXD .25W 1000 OHMS	IN					PPP4		N
29	C	24500074	300	PC	RES FXD .25W 3000 OHMS	IN					PPP4		N
28	C	24500094	400	PC	RES FXD .25W 20000 OHMS	IN					PPP4		N
34	C	24501806	100	IN	WIRE ELECT SOLID COPPER 24 GA	IN					PPP1		N
6	C	24505229	600	PC	CAP. FXD TANT 1 MF 35 VOLT	IN					PPP4		N
23	A	25175800	400	PC	DIODE(1N914)	IN							N
38	C	36143500	1700	PC	TRANSISTOR 2N3642	OUT	013252	041974			PPP4		N
37	B	38933500	100	PC	LABEL,IDENTIFICATION	IN							N
5	A	38958502	100	PC	TEST JACK, BLACK	IN							N
11	A	38958507	200	PC	TEST JACK, YELLOW	IN							N
12	A	38958509	100	PC	TEST JACK, PURPLE	IN							N
24	B	38991203	100	PC	PATCHCORD 1 IN. LG.	IN							N
35	A	39181003	100	IN	INSULATION, TEFLON, 24 AWG	IN	013256						N
13	B	39388300	100	PC	INT CKT 7400	IN							N
20	B	39389800	200	PC	INT CKT 74123	IN							N
36	A	39721800	REF	PC	ASSEMBLY REQUIREMENT	IN							N
3	C	39827500	200	PC	GUIDE,APPROACH	IN							N
38	A	50210500	1700	PC	TRANSISTOR 2N3642	IN	013252	041974					N
17	A	50250700	100	PC	I.C. TTL TRIPPLE 3 INPUT NAND	IN					PPP4		N
4	D	52936000	100	PC	AIR SEAL - 25 PAK	IN					PPP4		N
39	A	84905500	1700	PC	MTG PAD,TRANSISTOR	IN							N
33	A	84996708	100	PC	CAP, CER, 50 PF	IN							N
30	A	84996717	100	PC	CAP, CER, 220 PF	IN							N
31	A	84996721	200	PC	CAP, CER, 470 PF	IN							N
40	C	88788300	REF	PC	LOGIC DIAGRAM (4UZT)	IN							N
1	C	88800000	100	PC	PWB DIGITAL OUTPUT	IN							N
2	C	94243400	100	PC	CONNECTOR-CARD MTG 62 SOCKET	IN					PPP4		N
					NUMBER OF LINE ITEMS = 35								

PROJECT ENGINEER
R. DENGLER

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CLASSIFICATION NUMBER
88800105	E	CLA	D	PWA-DIG OUT TRUE=+28V LL(4UZT)	DS	IOM	04/12/74	

MF

PROCESSING DATE	PAGE NUMBER
07/30/74	~~2~~ 2

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD NUMBER	DATE EFFECTIVE	CLASSIFICATION NUMBER	OP NUMBER	MAKE/BUY PART TYPE	PN NC	S OR N

HIGHEST FIND NUMBER = 40

R. DENGLER

PROJECT ENGINEER

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RECYCLE FOR THE FUTURE

COMMENT SHEET

MANUAL TITLE CONTROL DATA® DA502-E, F, G, H, J, K Digital Output Unit Hardware Maintenance Manual

PUBLICATION NO. 88980300 REVISION A, B

FROM NAME: _____

BUSINESS ADDRESS: _____

COMMENTS: This form is not intended to be used as an order blank. Your evaluation of this manual will be welcomed by Control Data Corporation. Any errors, suggested additions or deletions, or general comments may be made below. Please include page number.

CUT ALONG LINE

STAPLE

STAPLE

FOLD

FIRST CLASS
PERMIT NO. 333

LA JOLLA, CA.

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CUT ALONG LINE

Test Set Up

FOLD

1544-4
Reset Low
Regen. High
Compl. Low
Mode AS.
A28+B28

1553-5
High
"
Ready High
Sync Hold
B28

STAPLE

STAPLE